MT6392 PMIC Datasheet

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Specifications are subject to change without notice.

Document Revision History

Revision	Date	Author	Description
1.0	2016-12-08	Chihao Chang	Initial Version

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1 Overview

1.1 Features

- Input range: 3.4 ~ 4.35V
- Three buck converters and 23 LDOs optimized for specific Tablet and portable systems
- Audio feature: high-power/quality audio amplifier
- 32K RTC oscillator for system timing, 1.8 and 2.8V clock buffer output
- SPI interface
- Li-ion battery charging function
- USB Battery Charging Specification ver1.1
- USB Type C Configuration Channel detection
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog Timer
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge

1.2 General Descriptions

MT6392 is a power management system chip optimized for tablet and other portable systems, containing three buck converters and 23 LDOs.

Sophisticated controls are available for power-up, battery charging and the RTC alarm. MT6392, optimized for maximum battery life, allows the RTC circuit to stay alive without a battery for several hours.

MT6392 adopts SPI interface and one SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and protocol for handshaking with BB.

MT6392 is available in a TFBGA 98L package. The operating temperature ranges from -30 to +85°C.

1.3 Applications

MT6392 is ideal for power management of tablet and other portable systems.

1.4 Ordering Information

Order #	Marking	Temp. range	Package
MT6392A/A		-30 ~ +85°C	TFBGA 98L

1.5 Top Marking Definition

MT6392A/A

YYWW: Date code
$: Random code

1.6 Pin Assignments and Descriptions

	1	2	3	4	5	6	7	8	9	10	11	
A	SPK_P	XOUT	XIN	INT	SPI_MISO	VDIG18	CHG_DP	VCORE_FB	GND_VCORE	VBAT_VCORE	VCORE_LX	A
B	SPK_N		GND		SPI_CSN	FSOURCE	CHG_DM	GND_VCORE_FB	GND_VCORE	VBAT_VCORE	VCORE_LX	B
C	VBAT_SPK		GND_SPK	GND	SPI_CLK	SPI_MOSI	VPROC_FB			VPROC_LX	VPROC_LX	C
D	VRTC28	WDTRSTB_IN	RTC32K_2V8		CLK_IN_26MHZ		GND_VPROC_FB		GND	VBAT_VPROC	VBAT_VPROC	D
E	INP	INN	SRCLKEN	RTC32K_1V8	GND		GND		GND	GND_VPROC	GND_VPROC	E
F	VCDT	BATON	EXT_PMIC_EN		GND	GND	GND	GND	GND	VSYS_LX	VSYS_LX	F
G	VREF_GND	VREF		GND		GND		VCN18			VBAT_VSYS	G
H	BATSNS	ISENSE	CHRLDO		VM25	VCN35		VCAMD	FCHR_ENB	AVDD22_BUCK	GND_VSYS	H
J	AVDD18_AUXADC	AVSS18_AUXADC			VEMC33			VCAM_IO	PWRKEY	RESETB	VM	J
K	TYPEC_CC1	TYPEC_CC2	VDRV	VCAM_AF	VELDO18	VMC	VADC18	VXO22	VAUD22	PMU_TESTMODE	VIO18	K
L	VUSB33	VGP2	VGP1	VBAT_LDOS3		VBAT_LDOS2	VIO28	VMCH	VCAMA	VBAT_LDOS1	VAUD28	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 1-1. MT6392 TFBGA 98L (5.6 x 5.6mm) pin assignment

Table 1-1. MT6392 pin descriptions

Ball	Pin Name	Type	Description
D10,D11	VBAT_VPROC	PWR	Power supply of VPROC
C10,C11	VPROC_LX	O	SW node of VPROC
E10,E11	GND_VPROC	GND	VPROC ground
C7	VPROC_FB	I	BUCK VPROC feedback pin
D7	GND_VPROC_FB	I	Remote sense on ground of VPROC
A10, B10	VBAT_VCORE	PWR	Power supply of VCORE
A11,B11	VCORE_LX	O	SW node of VCORE
A9,B9	GND_VCORE	GND	VCORE ground
A8	VCORE_FB	I	BUCK VCORE feedback pin
B8	GND_VCORE_FB	I	Remote sense on ground of VCORE
G11	VBAT_VSYS	PWR	Power supply of VSYS
F10,F11	VSYS_LX	O	SW node of VSYS
H11	GND_ VSYS	GND	VSYS ground
H10	AVDD22_BUCK	I	Power supply input of VSYSLDO
L10	VBAT_LDO1	PWR	Power supply input of LDO group1

Ball	Pin Name	Type	Description
L6	VBAT_LDO2	PWR	Power supply input of LDO group2
L4	VBAT_LDO3	PWR	Power supply input of LDO group3
K8	VXO22	O	VXO22 output voltage
G8	VCN18	O	VCN18 output voltage
H6	VCN35	O	VCN35 output voltage
L9	VCAMA	O	VCAMA output voltage
H8	VCAMD	O	VCAMD output voltage
J8	VCAMIO	O	VCAMIO output voltage
K4	VCAMAF	O	VCAMAF output voltage
L11	VAUD28	O	VAUD28 output voltage
K9	VAUD22	O	VAUD22 output voltage
K7	VADC18	O	VADC18 output voltage
J11	VM	O	VM output voltage
H5	VM25	O	VM25 output voltage
J5	VEMC33	O	VEMC33 output voltage
K6	VMC	O	VMC output voltage
L8	VMCH	O	VMCH output voltage
L1	VUSB33	O	VUSB33 output voltage
K11	VIO18	O	VIO18 output voltage
L7	VIO28	O	VIO28 output voltage
D1	VRTC28	O	RTC LDO output. Supply of RTC macro where backup battery can be added.
A6	VDIG18	O	VDIG18 output voltage
L3	VGP1	O	VGP1 output voltage
L2	VGP2	O	VGP2 output voltage
K5	VELDO18	O	VELDO18 output voltage
K3	VDRV	O	Charger current drive output
F1	VCDT	I	Fractional charger input voltage for charger detection
B7	CHG_DM	I	USB D- for BC1.1 standard
A7	CHG_DP	I	USB D+ for BC1.1 standard
H3	CHRLDO	O	CHRLDO output voltage
H2	ISENSE	I	Positive terminal for battery's charging current sensing resistor
H1	BATSNS	I	Negative terminal for battery's charging current sensing resistor
H9	FCHR_ENB	I	Force charging disable pin(Merge with HOMEKEY,Same as MT6323)

Ball	Pin Name	Type	Description
F2	BATON	I	Battery NTC pin for battery and its temperature sensing
K1	TYPEC_CC1	I	TYPEC input 1
K2	TYPEC_CC2	I	TYPEC input 2
E4	RTC32K_1V8	O	VIO18 domain 32kHz clock output
D3	RTC32K_2V8	O	VRTC domain 32kHz clock output
A3	XIN	IO	32K crystal connection port while using crystal to generate 32kHz clock
A2	XOUT	IO	32K crystal connection port while using crystal to generate 32kHz clock
C5	SPI_CLK	I	SPI control interface
B5	SPI_CSN	IO	SPI control interface
A5	SPI_MISO	IO	SPI control interface
C6	SPI_MOSI	IO	SPI control interface
D2	WDTRSTB_IN	I	Watchdog reset from AP
J10	RESETB	O	System reset release signal
E3	SRCLKEN	I	Source clock enable pin
F3	EXT_PMIC_EN	IO	Ext chip MT6311/MT6312 enable pin
G2	VREF	O	Bandgap reference voltage
G1	GND_VREF	GND	Ground for bandgap
B6	FSOURCE	PWR	EFUSE power source
K10	PMU_TESTMODE	I	PMU test mode signal (tied to GND in normal operation)
J9	PWRKEY	I	PWRKEY button
J1	AVDD18_AUXADC	PWR	1.8V power supply of AUXADC
J2	AVSS18_AUXADC	GND	AUXADC ground
C1	VBAT_SPK	PWR	Power supply of SPK
B1	SPK_N	O	Negative output of internal speaker amp
A1	SPK_P	O	Positive output of internal speaker amp
C3	GND_SPK	GND	GND of internal speaker amp
D5	CLK_IN_26MHZ	I	26MHz clock input
E2	INN	I	Audio negative input
E1	INP	I	Audio positive input
A4	INT	O	Default: Output 0 Interrupt to BB, high active
B3,C4,D9,E5,E7,E9,F5,F6,F7,F8,F9,G4,G6	GND	GND	Chip internal ground

2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 2-1. Absolute maximum ratings

Parameter	Conditions	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery Pin input voltage range				4.5	V
ESD robustness	HBM	2,000			V
Charger input withstand				30	V

2.2 Thermal Characteristics

Parameter	Conditions	Min.	Typical	Max.	Unit
Thermal resistance from junction to ambient	In free air		42.8[1]		°C/W

Note: The device is mounted on a 4-metal-layer PCB and modeled per JEDEC51-9 condition.

2.3 Pin Voltage Range

The table below lists operation range voltages for all MT6392 I/O pins.

Table 2-2. Pin voltage range

Ball	Pin Name	voltage	Unit
D10,D11	VBAT_VPROC	0 ~ 4.35	V
C10,C11	VPROC_LX	0 ~ 4.35	V
E10,E11	GND_VPROC	0	V
C7	VPROC_FB	0 ~ 4.35	V
D7	GND_VPROC_FB	0	V

Ball	Pin Name	voltage	Unit
A10, B10	VBAT_VCORE	0 ~ 4.35	V
A11,B11	VCORE_LX	0 ~ 4.35	V
A9,B9	GND_VCORE	0	V
A8	VCORE_FB	0 ~ 4.35	V
B8	GND_VCORE_FB	0	V
G11	VBAT_VSYS	0 ~ 4.35	V
F10,F11	VSYS_LX	0 ~ 4.35	V
H11	GND_ VSYS	0	V
H10	AVDD22_BUCK	0 ~ 2.42	V
L10	VBAT_LDO1	0 ~ 4.35	V
L6	VBAT_LDO2	0 ~ 4.35	V
L4	VBAT_LDO3	0 ~ 4.35	V
K8	VXO22	0 ~ 4.35	V
G8	VCN18	0 ~ 4.35	V
H6	VCN35	0 ~ 4.35	V
L9	VCAMA	0 ~ 4.35	V
H8	VCAMD	0 ~ 4.35	V
J8	VCAMIO	0 ~ 4.35	V
K4	VCAMAF	0 ~ 4.35	V
L11	VAUD28	0 ~ 4.35	V
K9	VAUD22	0 ~ 4.35	V
K7	VADC18	0 ~ 4.35	V
J11	VM	0 ~ 4.35	V
H5	VM25	0 ~ 4.35	V
J5	VEMC33	0 ~ 4.35	V
K6	VMC	0 ~ 4.35	V
L8	VMCH	0 ~ 4.35	V
L1	VUSB33	0 ~ 4.35	V
K11	VIO18	0 ~ 4.35	V
L7	VIO28	0 ~ 4.35	V
D1	VRTC28	0~3.08	V
A6	VDIG18	0 ~ 1.98	V
L3	VGP1	0 ~ 4.35	V
L2	VGP2	0 ~ 4.35	V
K5	VELDO18	0 ~ 4.35	V
K3	VDRV	0 ~ 4.35	V
F1	VCDT	0 ~ 1.8	V
B7	CHG_DM	0 ~ 4.35	V

Ball	Pin Name	voltage	Unit
A7	CHG_DP	0 ~ 4.35	V
H3	CHRLDO	0 ~ 3.08	V
H2	ISENSE	0 ~ 4.35	V
H1	BATSNS	0 ~ 4.35	V
H9	FCHR_ENB	0 ~ 4.35	V
F2	BATON	0 ~ 4.35	V
K1	TYPEC_CC1	0 ~ 3.63	V
K2	TYPEC_CC2	0 ~ 3.63	V
E4	RTC32K_1V8	0 ~ 1.98	V
D3	RTC32K_2V8	0~3.08	V
A3	XIN	0 ~ 3.08	V
A2	XOUT	0 ~ 3.08	V
C5	SPI_CLK	0 ~ 1.98	V
B5	SPI_CSN	0 ~ 1.98	V
A5	SPI_MISO	0 ~ 1.98	V
C6	SPI_MOSI	0 ~ 1.98	V
D2	WDTRSTB_IN	0 ~ 1.98	V
J10	RESETB	0 ~ 1.98	V
E3	SRCLKEN	0 ~ 1.98	V
F3	EXT_PMIC_EN	0 ~ 4.35	V
G2	VREF	0 ~ 1.32	V
G1	GND_VREF	0	V
B6	FSOURCE	0 ~ 1.98	V
K10	PMU_TESTMODE	0 ~ 4.35	V
J9	PWRKEY	0 ~ 4.35	V
J1	AVDD18_AUXADC	0 ~ 1.98	V
J2	AVSS18_AUXADC	0	V
C1	VBAT_SPK	0 ~ 4.35	V
B1	SPK_N	0 ~ 4.35	V
A1	SPK_P	0 ~ 4.35	V
C3	GND_SPK	0	V
D5	CLK_IN_26MHZ	0 ~ 1.98	V
E2	INN	0 ~ 4.35	V
E1	INP	0 ~ 4.35	V
A4	INT	0 ~ 1.98	V
B3,C4,D9,E5,E, E9,F5,F6,F7,F8, F9,G4,G6	GND	0	V

2.4 Recommended Operating Range

Table 2-3. Operating conditions

Parameter	Conditions	Min.	Typical	Max.	Unit
Operating temperature range		-30		85	°C

2.5 Electrical Characteristics

VBAT = 2.5V ~ 4.35V, minimum loads applied on all outputs, unless otherwise noted.

Typical values are at T_A = 25°C.

Table 2-4. General electrical specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Operation Ground Current					
Off mode with 32K crystal	VBAT=4.35V, Temp=25°C			50	µA
Off mode w/o 32K crystal	VBAT=4.35V, Temp=25°C			65	uA
Suspend mode with 32K crystal	VBAT=4.35V, Temp=25°C			300	uA
Suspend mode w/o 32K crystal	VBAT=4.35V, Temp=25°C			315	uA
Under Voltage Lockout (UVLO)					
Under voltage falling threshold (UVLO_VTHL)		2.75	2.9	3.05	V
Under voltage rising threshold (UVLO_VTHH)		3.05	3.2	3.35	V
Threshold voltage accuracy		-150		+150	mV
Deep Discharge Lockout (DDLO)					
Deep discharge falling threshold (DDLO_VTHL)		2.35	2.5	2.65	V
Deep discharge rising threshold (DDLO_VTHH)		2.55	2.7	2.85	V
Threshold voltage accuracy		-150		+150	mV
Reset Generator					
Output high		VIO-0.4			V
Output low				0.2	V

Output current (Ioh)	Vo > VIO-0.4V		1		mA
Delay time from VUSB33 turn on to RESETB release			44		ms
Interrupt					
Output high		VIO-0.4			V
Output low				0.2	V
PWRKEY/FCHR_ENB					
High voltage		0.7*VBAT			V
Low voltage				0.3*VBAT	V
De-bounce time			50		ms
Control Input Voltage					
Control input high (SPI, SRCLKEN related)		0.7*VIO			V
Control input low (SPI, SRCLKEN related)				0.3*VIO	V
Thermal Shut-down					
PMIC shut-down threshold			150		°C
Shut-down release threshold			105		°C

2.6 Regulator Output

Table 2-5. Buck specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Buck – VPROC					
Turn-on overshoot	Vout=1.15V No load			10	%
Short current		Imax*1.1		Imax*5.0	
Temperature coefficient	Vbat=3.8V I_Load=No Load	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=1.15V, L_DCR=60mΩ I_Load=100mA		82		%
	Vbat=3.8V, Vout=1.15V, L_DCR=60mΩ I_Load=500mA		84		%
	Vbat=3.8V, Vout=1.15V, L_DCR=60mΩ I_Load=1000mA		79		%
	Vbat=3.8V, Vout=1.15V,		54		%

Parameter	Conditions	Min.	Typical	Max.	Unit
	L_DCR=60mΩ I_Load=3100mA				
Soft start	Vout=1.15V No load			1000	us
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			15	mVpp
Load transient (PWM)	Vbat=3.8V IOUT = 1.2A to 3.1A (Tr/Tf = 1us)	-4		+4	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.4V to 4.5V I_Load=10mA to Imax	-1		+1	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.4V to 4.5V I_Load=0~10mA	-1		+3	%
Buck – VCORE					
Turn-on overshoot	Vout=1.15V No load			10	%
Short current		Imax*1.2		Imax*5.0	
Temperature coefficient	Vbat=3.8V I_Load=No Load	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=1.15V, L_DCR=60mΩ I_Load=100mA		82		%
	Vbat=3.8V, Vout=1.15V, L_DCR=60mΩ I_Load=500mA		84		%
	Vbat=3.8V, Vout=1.15V, L_DCR=60mΩ I_Load=1000mA		79		%
	Vbat=3.8V, Vout=1.15V, L_DCR=60mΩ I_Load=2800mA		58		%
Soft start	Vout=1.15V No load~10mA			1000	us
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			15	mVpp

Parameter	Conditions	Min.	Typical	Max.	Unit
Load transient (PWM)	Vbat=3.8V IOUT = 0.8A to 2.8A (Tr/Tf = 1us)	-4		+4	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.4V to 4.5V I_Load=10mA to Imax	-1		+1	%
DC accuracy (Included Line/Load regulation @PFM)	VBAT=3.4V to 4.5V I_Load=0~10mA	-1		+3	%
Buck – VSYS					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*5	A
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax/ 1.0*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=2.2V, L_DCR=35mΩ I_Load=1mA		70		%
	Vbat=3.8V, Vout=2.2V, L_DCR=35mΩ I_Load=100mA		82		%
	Vbat=3.8V, Vout=2.2V, L_DCR=35mΩ I_Load=500m A		78		%
	Vbat=3.8V, Vout=2.2V L_DCR=35mΩ I_Load=700mA		70		%
Soft start	No load			1	ms
Output ripple voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient	Vbat=3.8V IOUT = 0<–>150 mA. IOUT = 50mA<–>250 mA. IOUT = 150mA<–>750mA (Tr/Tf = 1.5 uS)	-4.0		+4.0	%
DC accuracy (Included Line/Load regulation @PWM)	VBAT=3.4V to 4.5V I_Load=transient point to Imax	-1.0		+1.0	%
DC accuracy	VBAT=3.4 to 4.5V	-1.0		+2.0	%

Parameter	Conditions	Min.	Typical	Max.	Unit
(Included Line/Load regulation @PFM)	I_Load=0~ transient point				

Table 2-6. LDO specifications

Parameter	Type	Conditions		Min.	Typ.	Max.	Unit
All test condition for input power range	ALDO and DLDO for VBAT range	(note#1) Min spec: max{Output Voltage +0.35V; VBAT≧3.4}		(note #1)		4.5	V
	VSYSLDO for AVDD22_BUCK range	(note#2) Min spec: max{Output Voltage +0.35V; AVDD22_BUCK≧2.2*0.99}		(note #2)		2.2*1.01	V
Overall DC voltage accuracy	VXO22, VADC18, VCN35, VIO28, VUSB33, VMC, VMCH, VEMC33, VCAM_AF, VGP1, VGP2, VELDO18, VDIG18, VCAM_IO	Iout= 0~0.8*Imax	1. Input power range 2. Typical capacitor 3. TA= -30°C ~+85°C	-5		+5	%
	Other LDOs			-2.5		+2.5	%
	Low power mode for ALDO, DLDO and SLDO	Iout= 0~0.05*Imax	1. Input power range 2. Typical capacitor 3. TA= -30°C ~+85°C	-5		+5	%
Load/Line regulation	Normal mode for ALDO, DLDO and SLDO	Iout= 0~Imax	1. Input power range 2. Typical capacitor 3. TA= 25°C	-1.5		+1.5	%
	VRTC and VDIG18	Iout= 0~0.3*Imax		-5		+5	%
	Low power mode for ALDO, DLDO and SLDO	Iout= 0~0.05*Imax		-5		+5	%
Power Off Voltage	ALDO, DLDO and SLDO	1. Input power range 2. Typical capacitor 3. TA= -30°C ~+85°C 4. Iout= 0mA				0.1	V
Temperature	ALDO, DLDO and	1. Input power range		-100		100	ppm/

Parameter	Type	Conditions		Min.	Typ.	Max.	Unit
coefficient	SLDO	2. Typical capacitor 3. TA= -30°C ~+85°C 4. Iout= 0 mA					C
Load transient response	ALDO, DLDO and SLDO	Slew rate= 15mA/us	1. Input power range 2. Typical capacitor 3. TA= -30°C ~+85°C 4. Iout= 0.01*Imax~0.5 *Imax	-5		+5	%
	VCN35, VEMC33, VCN18, VM	Slew rate= 0.25*Imax/us		-5		+5	%
Turn-on rise time	ALDO, DLDO and SLDO	1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout= 0mA		20		300	us
Turn-on overshoot	ALDO, DLDO and SLDO	1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout= 0mA				Vout* 1.1	V
Power off Time	ALDO, DLDO and SLDO	Bypass capacitor ≦ 2.2uF	1. Input power range 2. TA= +25°C 3. Iout= 0mA			4	ms
		Bypass capacitor ≦ 4.7uF				8	ms
		Bypass capacitor ≦ 10uF				12	ms
Output noise	ALDO	Freq = 10Hz to 80kHz	1. Input power range 2. Typical capacitor 3. TA= +25°C 4. Iout=0.2*Imax ~0.5*Imax		90		uVrms
	DLDO and SLDO				500		uVrms
	ALDO, DLDO and SLDO	Freq = 10Hz to 10MHz			1000		uVrms
PSRR	ALDO	Freq = 217Hz to 3kHz	1. Input power range		65		dB

Parameter	Type	Conditions		Min.	Typ.	Max.	Unit
		Freq= 3kHz to 30kHz	2. Typical capacitor 3. TA= +25°C 4. Iout= 0.2*Imax / 0.5*Imax		45		dB
	DLDO and SLDO	Freq = 217Hz			40		dB
Short current	ALDO, DLDO and SLDO	OC	1. Input power range 2. Typical capacitor 3. TA= +25°C	1.2 x Imax		5 x Imax	
Normal mode quiescent current	VM	1. Input power range 2.Typical capacitor 3. TA= +25°C 4. Iout= 0mA			1000		uA
	VCAMA				300		
	VCN35, VMCH, VEMC33				70		
	Other LDOs				55		
	VRTC and VDIG18				10		
Low power mode quiescent current	VAUD28, VXO22, VCN35, VIO28, VUSB33, VMC, VMCH, VEMC33, VCAM_AF, VGP1, VGP2, VELDO18, VM25, VM, VIO18, VCN18, VCAMD				15		
	Other LDOs				10		

2.7 Audio AMP

Table 2-7. Class AB/D audio amplifier specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Class AB audio amplifier					
RMS power	8Ω load, VBAT = 4.2V THD + N = 1%		850		mW

Parameter	Conditions	Min.	Typ.	Max.	Unit
	8Ω load, VBAT = 3.8V THD + N = 1%		700		mW
	8Ω load, VBAT = 3.4V THD + N = 1%		600		mW
	8Ω load, VBAT = 4.2V THD + N = 10%		N/A		mW
	8Ω load, VBAT = 3.8V THD + N = 10%		N/A		mW
	8Ω load, VBAT = 3.4V THD + N = 10%		N/A		mW
THD+N	1kHz, Po = 0.5Wrms, VBAT = 4.2V		0.05	0.2	%
	1kHz, Po = 0.4Wrms, VBAT = 3.8V		N/A	N/A	%
	1kHz, Po = 0.3Wrms, VBAT = 3.4V		N/A	N/A	%
PSRR	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 4.2V		N/A		dB
	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		75		dB
	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.4V		N/A		dB
	1kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		75		dB
	4kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		75		dB
	20kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		50		dB
Noise level	VBAT = 4.2V, 12dB gain 8Ω, A-weighted		N/A		µV
	VBAT = 3.4V, 12dB gain 8Ω, A-weighted		N/A		uV
	VBAT = 4.2V, 0dB gain		N/A	100	µV

Parameter	Conditions	Min.	Typ.	Max.	Unit
	8Ω, A-weighted				
	VBAT = 3.4V, 0dB gain 8Ω, A-weighted		N/A		uV
	VBAT = 4.2V, -6dB gain 8Ω, A-weighted		N/A		µV
	VBAT = 3.4V, -6dB gain 8Ω, A-weighted		N/A		uV
Gain adjustment		6		15	dB
Gain adjustment steps			1		dB
Quiescent current	No load, VBAT=4.2V		3	6	mA
	No load, VBAT=3.8V		3	6	mA
	No load, VBAT=3.4V		3	6	mA
DC offset	VBAT = 4.2V, 12dB gain		N/A		mV
	VBAT = 3.8V, 12dB gain		N/A		mV
	VBAT = 3.4V, 12dB gain		N/A		mV
	VBAT = 4.2V, 0dB gain		N/A		mV
	VBAT = 3.8V, 0dB gain		N/A		mV
	VBAT = 3.4V, 0dB gain		N/A		mV
	VBAT = 4.2V, -6dB gain		N/A	N/A	mV
	VBAT = 3.8V, -6dB gain		N/A	N/A	mV
	VBAT = 3.4V, -6dB gain		N/A	N/A	mV
Class D audio amplifier					
RMS power	8Ω load, VBAT = 4.2V THD + N = 1%		850		mW
	8Ω load, VBAT = 3.8V THD + N = 1%		700		mW
	8Ω load, VBAT = 3.4V THD + N = 1%		600		mW
	8Ω load, VBAT = 4.2V THD + N = 10%		N/A		mW
	8Ω load, VBAT = 3.8V THD + N = 10%		N/A		mW
	8Ω load, VBAT = 3.4V THD + N = 10%		N/A		mW
THD+N	1kHz, Po = 0.5Wrms, VBAT = 4.2V		N/A	0.2	%
	1kHz, Po = 0.4Wrms, VBAT = 3.8V		N/A	N/A	%
	1kHz, Po = 0.3Wrms,		N/A	N/A	%

Parameter	Conditions	Min.	Typ.	Max.	Unit
	VBAT = 3.4V				
PSRR	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 4.2V		N/A		dB
	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		N/A		dB
	217Hz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.4V	65	75		dB
	1kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		75		dB
	4kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		75		dB
	20kHz, Vin = 200mVpk-pk Input AC to ground, VBAT = 3.8V		50		dB
Noise level	VBAT = 4.2V, 12dB gain 8Ω, A-weighted		N/A		μV
	VBAT = 3.4V, 12dB gain 8Ω, A-weighted		N/A		uV
	VBAT = 4.2V, 0dB gain 8Ω, A-weighted		N/A	100	μV
	VBAT = 3.4V, 0dB gain 8Ω, A-weighted		N/A	100	uV
Efficiency	VBAT = 4.2V 0.8W, 8Ω with 68uH, 1kHz	80	85		%
	VBAT = 4.2V 0.5W, 8Ω with 68uH, 1kHz		N/A		%
	VBAT = 3.8V 0.5W, 8Ω with 68uH, 1kHz		N/A		%
	VBAT = 3.4V 0.5W, 8Ω with 68uH, 1kHz		N/A		%
Gain adjustment		6		15	dB
Gain adjustment steps			1		dB
Quiescent current	No load, VBAT=4.2V		4	6	mA
	No load, VBAT=3.8V		4	6	mA

Parameter	Conditions	Min.	Typ.	Max.	Unit
	No load, VBAT=3.4V		4	6	mA
DC offset	VBAT = 4.2V, 12dB gain			N/A	mV
	VBAT = 3.8V, 12dB gain			N/A	mV
	VBAT = 3.4V, 12dB gain			N/A	mV
	VBAT = 4.2V, 0dB gain		N/A		mV
	VBAT = 3.8V, 0dB gain		N/A		mV
	VBAT = 3.4V, 0dB gain		N/A		mV

2.8 Battery Charger

Table 2-13. Charger specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
CHRIN operating voltage		4	5	10.5	V
OTG B-Valid detection		0.8	2.4	4	V
VCDT detection threshold	VCDT_VTHL[3:0] = 0000 ~ 1111	4		10.5	V
HV adaptive current @ pre_charge	CHRIN switch threshold (300mA => 70mA)		7		V
	CHRIN switch threshold (70mA => 300mA)		6		V
VBAT CC voltage accuracy	Programmable: 3.3~3.45, 50mV steps	-70		+70	mV
VBAT CV voltage accuracy	Programmable: 3.775~4.425 V	-50		+50	mV
VBAT OV voltage accuracy	Programmable: 3.8~4.45 V	-50		+50	mV
CC mode charging current accuracy	Programmable:450 ~1600 mA (Rsense=200mΩ)	-10		+10	%

2.9 BC1.x

Table 2-8. BC1.x specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
BC11 charging port detection (Pre-CC current)	Standard down-stream port		70		mA
	Standard charging down-stream port		70		mA
	DP, DM short		300		mA
	DP, DM floating		300		mA

Parameter	Conditions	Min.	Typical	Max.	Unit
BC11 characteristics	IPU_DP, IPU_DM	7	9.6	13	uA
	IPD_DP, IPD_DM	50	96	150	uA
	VSRC on DP, DM	500	630	700	mV
	Current pulse value under 2.2V		70		mA
	Current pulse period under 2.2V		550		ms

2.10 Down Load Without Battery

Table 2-9. Download without batteryspecifications

Parameter	Conditions	Min.	Typical	Max.	Unit
USBDL	Duration		32.0		s
	Current		450		mA

2.11 AUXADC

Table 2-10. AUXADC specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply voltage		-	1.8	-	V
Resolution	Channel 0,1,7	-	-	15	Bits
	Others	-	-	12	Bits
Analog-input bandwidth			50K		Hz
Sample rate			100K		Hz
Offset error	Relative to full-scale	-1	-	+1	%
Gain error	Relative to full-scale	-1	-	+1	%
INL	15-bit output		2		LSB
DNL	15-bit output		2		LSB

2.12 Type-C

Parameter	Conditions	Min.	Typical	Max.	Unit
R_Pull Down	VUSB>2.93V	-10%	5.1K	10%	Ω
R_Pull Down	VUSB<2.93V, CC pin voltage > 1V	-20%	5.1K	20%	Ω

Parameter	Conditions	Min.	Typical	Max.	Unit
I_Pull up	VUSB>2.93V	-20%	80	20%	uA
I_Pull up	VUSB>2.93V	-8%	180	8%	uA
I_Pull up	VUSB>2.93V	-8%	330	8%	uA
zOPEN	VUSB>2.93V ,Minimum Impedance to GND	126k			Ω
CC Detection threshold	Default USB Power	0.18	0.2	0.22	V
CC Detection threshold	USB Type-C Current @3 A	0.66	0.68	0.70	V
CC Detection threshold	USB Type-C Current @ 1.5 A	1.26	1.28	1.30	V
Threshold. (UFP attach VTH and INT out)		0.18	0.2	0.22	V
Threshold. (DFP attach VTH and INT out)		2.58	2.6	2.62	V
Standby current	DRP(50%)			12	uA
USB33_RDY_V43 power good	Power good for Type C block(Vbat rising)	2.86	2.93	3.0	V
	Power good for Type C block(Vbat falling)	2.8	2.87	2.94	V

3 Functional Description

3.1 General Description

MT6392 is a fully integrated PMIC targeted for tablet and other portable systems power providers. The MT6392 PMIC block diagram is shown here.

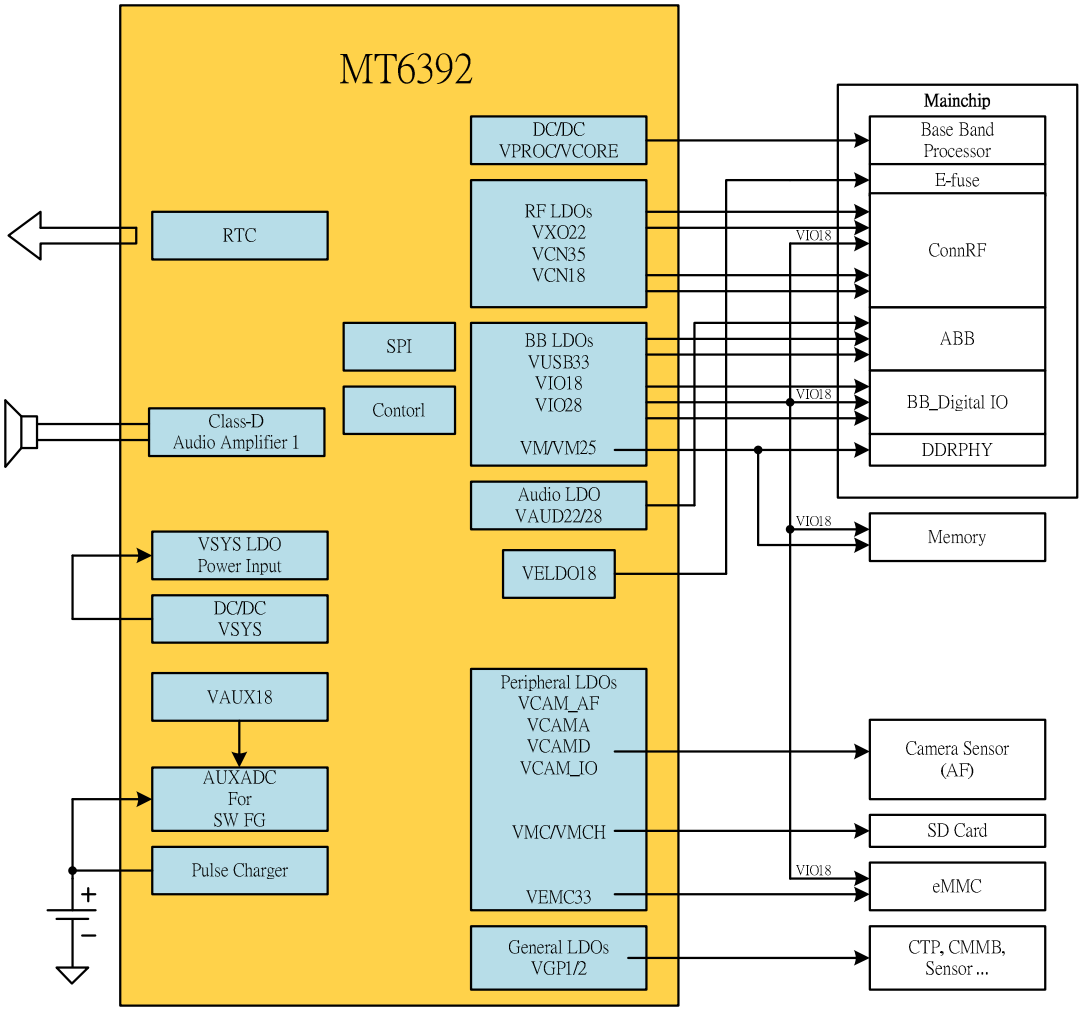

Figure 3-1. MT6392 block diagram

MT6392 manages the power supply of the baseband processor, memory, camera and SD card, etc. MT6392 includes the following analog functions for use on tablets and other portable systems.

- LDO and BUCK: Provides regulated lower output voltage level from Li-Ion battery

- AUXADC: 15 bits of analog to digital converter for thermal/accessory detection monitor and measurement
- Controller: Generates power-on/off sequence, system reset and exceptional handling function
- Charger controller: Controls/Protects battery charging procedure
- High-quality audio feature: Supports high-power/quality audio amplifier
- Fuel gauge: Supports accurate battery capacity monitor

More detailed descriptions of each sub-block are provided in the following sections.

3.2 Power-On/Off Sequence

PMIC handles the power-on and power-off of the handset. If the battery voltage is neither in the UVLO state (VBAT < UVLO_VTHH) nor in the thermal condition, there are three methods to power on the handset system.

- Pulling PWRKEY low (User presses PWRKEY.)
- Valid charger plug-in
- Setting BBWAKEUP high

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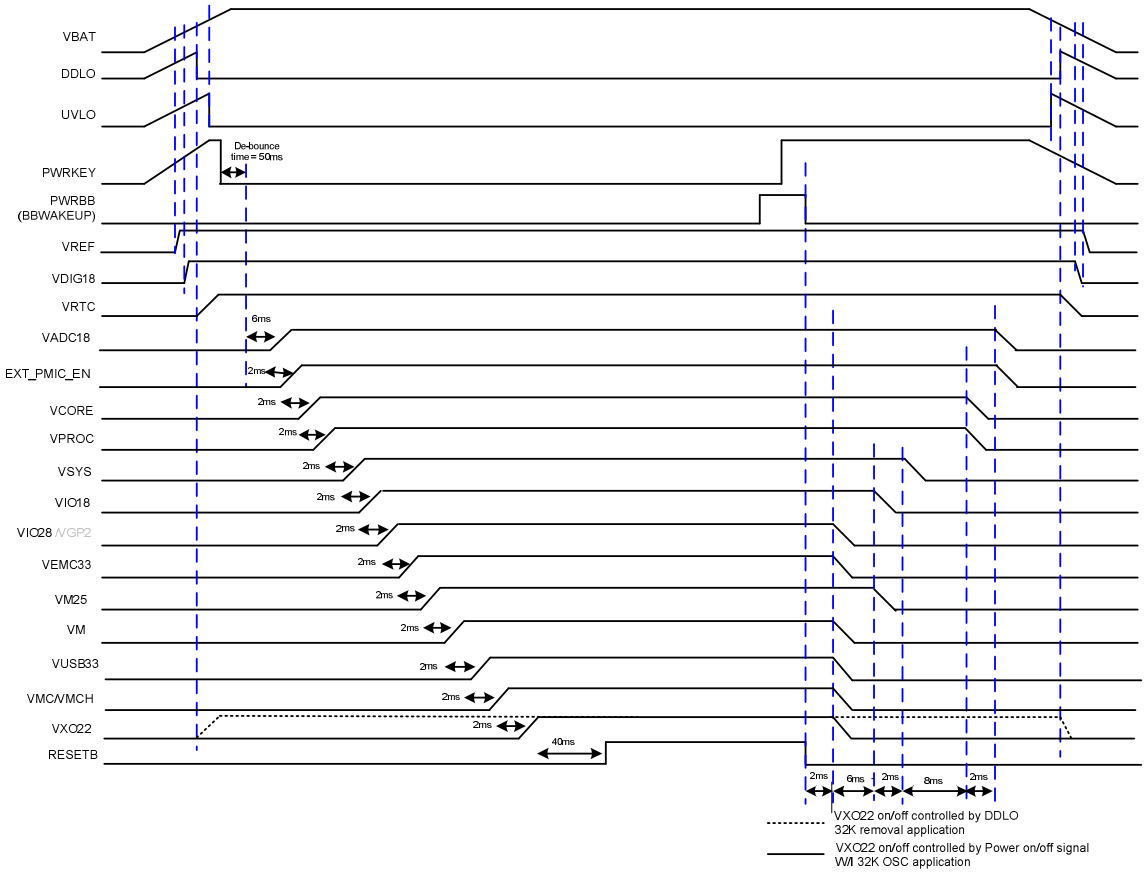


Figure 3-2. Power-on/off control sequence with XTAL by pressing PWRKEY

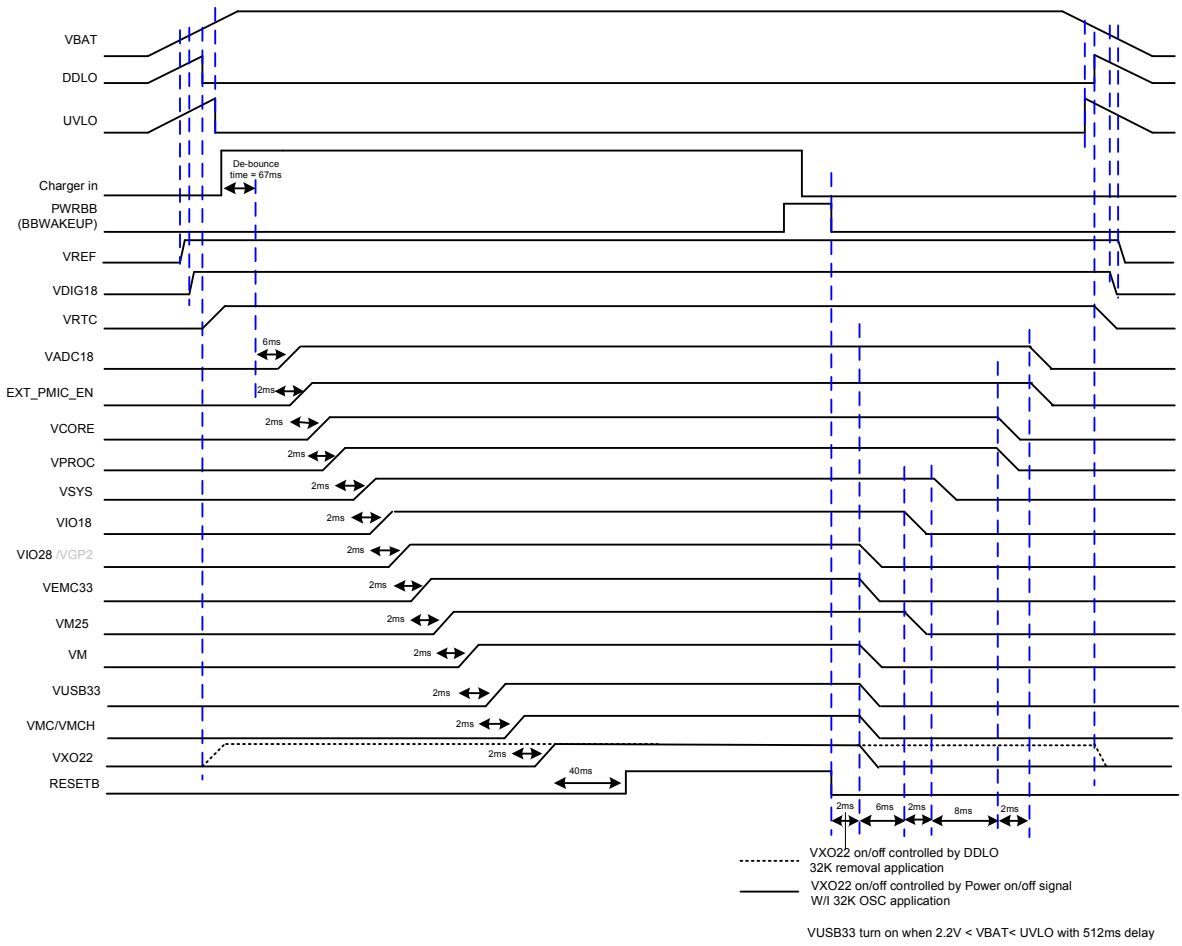


Figure 3-3. Power-on/off control sequence with XTAL by charger plug in

- Pressing PWRKEY (pulling the PWRKEY pin to low level)
- Pulling PWRKEY low is a typical method to turn on the handset. The system reset ends at the moment when all default-on regulators are sequentially turned on. After that, the baseband will send the BBWAKEUP signal back to PMIC for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMIC receives BBWAKEUP from the baseband.

The RTC module generates BBWAKEUP to wake up the system. If the RTC module is scheduled to wake up the handset at some time, the BBWAKEUP signal will be directly sent to PMIC. In this case, BBWAKEUP becomes high at specific moment and allows PMIC power-on. This is called the RTC alarm.

Valid charger plug-in (CHRIN voltage within valid range)

The charger plug-in will also turn on the handset if the charger is valid. When CHRIN input voltage> CHRIN_LV_VTH and V_{BATSYS}>UVLO_VTHH, the handset will also be powered on.

3.3 Under-Voltage Lockout (UVLO)

The UVLO state in PMIC prevents start-up if the initial voltage of the main battery is below UVLO_VTH. The judgment is done by VSYSNS (with charger plugged in) and VBATSNS+VSYSNS (without charger plugged in). It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state and PMIC will be turned off by itself, except for VRTC LDO, to prevent further discharging. Once PMIC enters the UVLO state, it will draw low quiescent current. RTC LDO will still be working until DDLO disables it.

Deep discharge lockout (DDLO)
PMIC will enter the deep discharge lockout (DDLO) state when the battery voltage drops below DDLO_VTHL. In this state, VRTC LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or even damage to the cells.

Reset
PMIC contains a reset control circuit which takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter, which uses the clock from the internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection
If the die temperature of PMIC exceeds 150°C, PMIC will automatically disable all regulators except for VRTC. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the regulators.

3.4 Buck Converter and Application Reference

There are three buck converters in MT6392 to efficiently generate regulated power for processor, digital core and system LDO. (Refer to the block diagram shown in Figure 3-1 above.) The buck converters operate with typically 3MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the converter automatically enters pulse frequency modulation (PFM) mode to save power and improve light load efficiency. It also has a force-PWM mode option to allow the converter to remain in the PWM mode regardless of the load current, so that the noise spectrum of the converter can be minimized for certain highly-noise-sensitive handset applications. The buck converters also have an internal over-current protection (OCP) circuit to limit the maximum high-side power FET current in over-load conditions. It has an internal soft start circuit to control the ramp-up rate of the output voltage during start-up.

Table 3-1. Buck converter brief specifications

BUCK name	Default voltage (V)	Vout (Volt)	Voltage step (mV)	Imax (mA)	Default on (Y/N)	Application
VCORE	1.15	0.7 ~ 1.4	6.25	2800	Y	Digital core always
VPROC	1.15	0.7 ~ 1.4	6.25	3100	Y	PROCESSOR
VSYS	2.2	2.2	12.5	1,400	Y	System LDO input

3.5 Low Dropout Regulator (LDOs) and Application Reference

Table 3-2. LDO types and brief specifications

Type	LDO name	Input power domain	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
ALDO	VAUD28	VBAT_LDOS1	2.8	2.8	150	N	Audio
ALDO	VXO22	VBAT_LDOS1	2.2	2.2	20	Y	DCXO
ALDO	VAUD22	VBAT_LDOS1	2.2	1.8/1.9/2.0/ 2.2	40	N	Audio
ALDO	VADC18	VBAT_LDOS1	1.8	1.8	10	Y	AUXADC
ALDO	VCAMA	VBAT_LDOS1	2.8	2.8	150	N	Camera
DLDO	VCN35	VBAT_LDOS2	3.5	3.3/3.4/3.5/ 3.6	350	N	WCN
DLDO	VIO28	VBAT_LDOS2	2.8	2.8	200	Y	IO pad power
DLDO	VUSB33	VBAT_LDOS3	3.3	3.3	40	Y	USB
DLDO	VMC	VBAT_LDOS2	3.3	1.8/3.3	100	Y	SD card
DLDO	VMCH	VBAT_LDOS2	3.3	3.0/3.3	400	Y	SD card
DLDO	VEMC33	VBAT_LDOS3	3.3	3.0/3.3	400	Y	EMMC
DLDO	VCAM_AF	VBAT_LDOS3	2.0	1.2/1.3/1.5/ 1.8/2.0/2.8/ 3.0/3.3	100	N	Camera
DLDO	VGP1	VBAT_LDOS3	2.8	1.2/1.3/1.5/ 1.8/2.0/2.8/ 3.0/3.3	100	N	General purpose LDO

Type	LDO name	Input power domain	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
DLDO	VGP2	VBAT_LDOS3	2.8	1.2/1.3/1.5/ 1.8/2.0/2.8/ 3.0/3.3	100	N	General purpose LDO
DLDO	VELDO18	VBAT_LDOS2	1.8	1.8/2.0	50	N	Efuse
DLDO	VM25	VBAT_LDOS3	2.5	2.5	100	Y	Memory power
DLDO	VDIG18	VBAT_LDOS2	1.8	1.8	20	Y	PMIC digital
VSYS LDO	VM	AVDD22_BUCK	1.24	1.24/1.39	700	Y	Memory power
VSYS LDO	VIO18	AVDD22_BUCK	1.8	1.8	300	Y	IO pad power
VSYS LDO	VCN18	AVDD22_BUCK	1.8	1.8	120	N	WCN
VSYS LDO	VCAMD	AVDD22_BUCK	1.2	1.2/1.3/1.5/ 1.8	150	N	Camera
VSYS LDO	VCAM_IO	AVDD22_BUCK	1.8	1.8	100	N	Camera
RTCLDO	VRTC	VBAT_LDOS1	2.8	2.8	2	Y	Real-time clock

3.6 Class-AB/D Audio Amplifier

MT6392 has built-in one channel high efficiency class AB/D audio power amplifier capable of delivering 0.7 watt of power on an 8 ohm BTL load from a 3.8V battery supply. Over-current protection for both class-AB and class-D modes are integrated. The amplifier receives analog audio input signals. The block diagram is shown below.

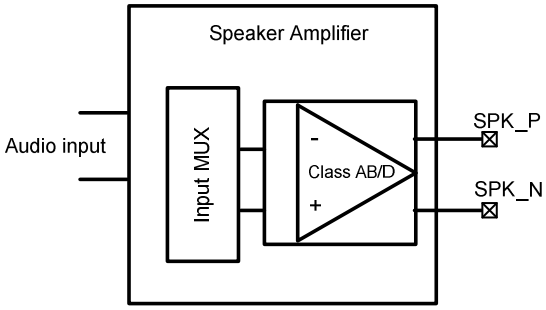


Figure 3-8. Class-AB/D Block Diagram

3.7 Battery Charger (Charger Controller)

The charger controller senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process will be activated.

3.7.1 Pulse Charger (PCHR)

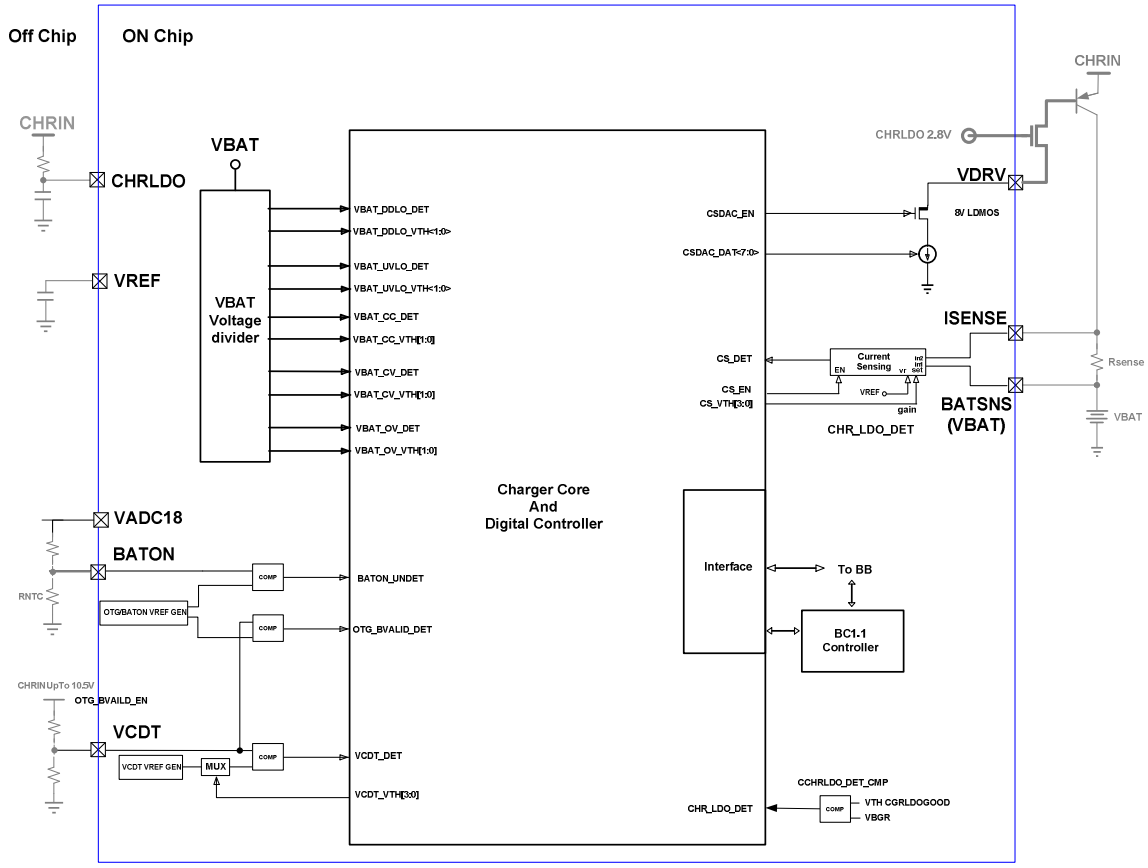


Figure 3-4. PCHR Block Diagram

3.7.2 Charger Detection

Whenever an invalid charging source is detected (> 7.0V), the charger detector will stop the charging process immediately to avoid burning out the chip or even the mobile device. Furthermore, if the charger-in level is not high enough (< 4.3V), the charger will also be disabled to avoid improper charging behavior.

3.7.3 Charging Control

When the charger is active, the charger controller will manage the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger supports pre-charge mode (VBAT < 3.2V, PMIC power-off state), CC mode (constant current mode or fast charging mode at the range of 3.2V < VBAT < 4.2V) and CV mode (constant voltage mode) to optimize the charging procedure for Li-ion battery. See the figure below for the charging state diagram.

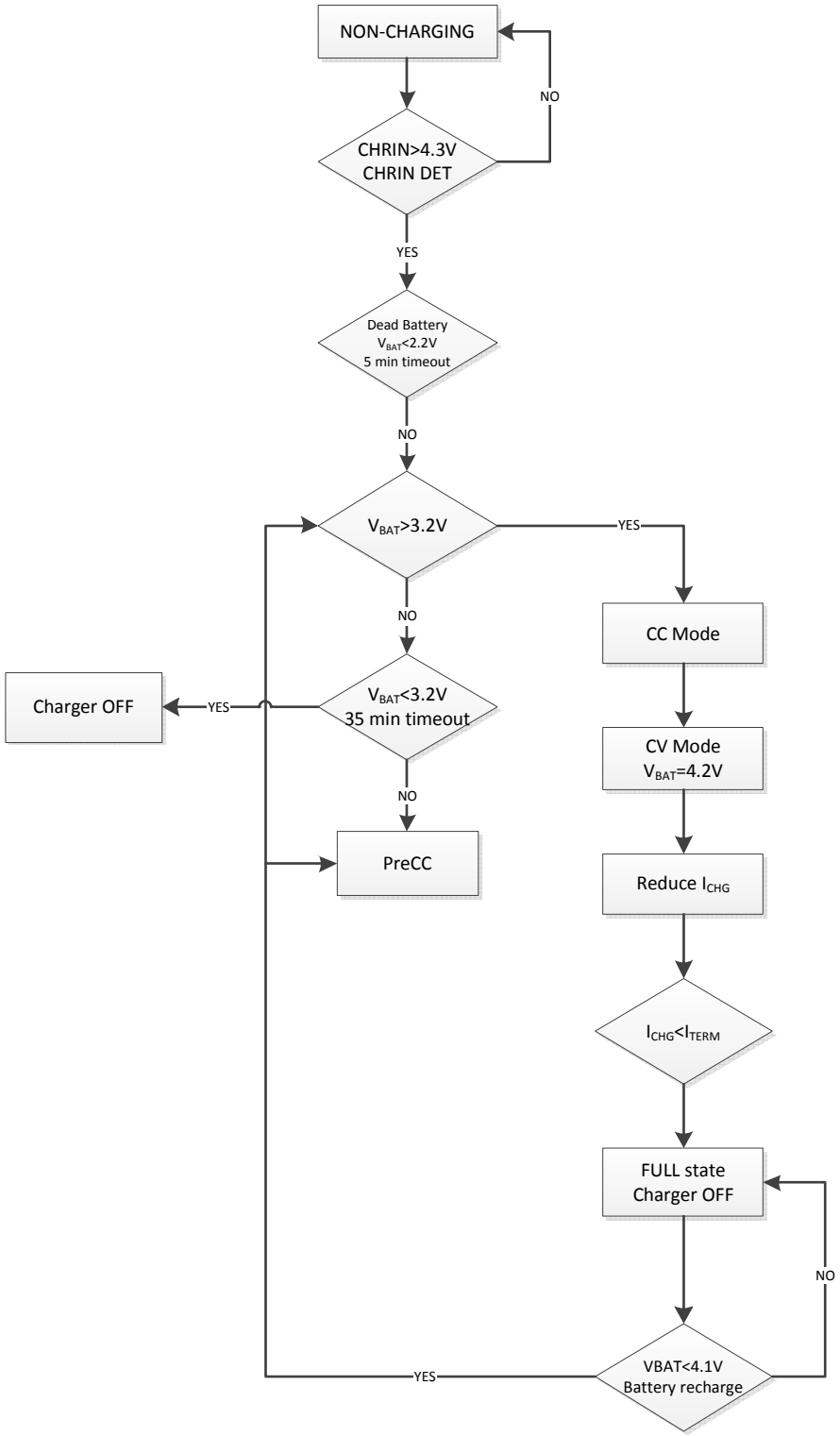


Figure 3-5. Charging States Diagram

3.7.4 Pre-Charge Mode

When the battery voltage is in the UVLO state, the charger will operate in the pre-charge mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2.2V, IUNIT trickle charging current is applied to the battery.

The IUNIT trickle charging current is about 550ms pulse 70mA current when VBAT is under 2.2V.

When the battery voltage exceeds 2.2V, i.e. the PRECC1 stage, the closed-loop pre-charge will be enabled. The voltage drop across the external RSENSE is kept around 60mV (AC charger) or 14mV (USB host). The closed-loop pre-charge current can be calculated:

$$I_{PRECC1,AC\,adapter} = \frac{V_{SENSE}}{Rsense} = \frac{60mV}{Rsense}$$

$$I_{PRECC1,USB\,HOST} = \frac{V_{SENSE}}{Rsense} = \frac{14mV}{Rsense}$$

3.7.4.1 Constant Current Mode

As the battery is charged up and over 3.2V, it can switch to the CC mode. (CHR_EN should be high) In the CC mode, several charging currents can be set by programming registers or the external RSENSE resistor. The charging current can be determined by CS_VTH/RSENSE, where CS_VTH is programmed by registers. For example, if RSENSE is selected as 0.2ohm, the CC mode charging current can be set from 70 to 1,600mA. It can accommodate the battery charger to various charger inputs with different current capability.

Constant-voltage mode and over-voltage protection (OV)

While the battery voltage reaches about 4.2V, a constant voltage is used for charging. This is called the full-voltage charging mode or constant-voltage charging mode in correspondence to a linear charger. While the battery voltage actually reaches 4.2V, the charging current is gradually decreased step-by-step, the end-of-charging process starts. It may prolong the charging and detecting period for acquiring optimized full charging volume. The charging process is completed once the current reaches zero automatically and this mechanism is optimized for different battery packs. Whenever the battery voltage exceeds 4.3V (programmed by SW), a hardware OV protection is activated and turns off the charger immediately.

3.7.4.2 BC1.1 Dead-Battery Support

MT6392 also supports dead-battery condition BC1.1. These specifications protect dead-battery charging by timer and trickle current. Once the battery voltage is below 2.2V, a period (TUNIT) of trickle current (IUNIT) will be applied to the battery.

If the battery voltage is still below 2.2V after applying the trickle current, the charger will be disabled. On the other hand, once the battery voltage rises up to above 2.2V, the charger will enter the PRECC1 stage, and the charging current will be 70mA or 300mA depending on the type of the charging port.

When the battery is below 3.2V, the charger will charge the battery with the PRECC1 current.

A dedicated 5-min (T1) timer will be timed out and disable the charger if the battery voltage is always below 2.7V under charging. Another 35-min (T2) timer will also be timed out and disable the charger if the battery voltage is always kept between 2.7V and 3.2V under charging.

The trickle current (IUNIT) and two dedicated timers protect the charging action if the battery is dead.

3.7.4.3 Auto Power-On Mode (USB DL without Battery)

MT6392 features default auto power-on mode (or USB DL without battery) no matter with or without battery. You can disable auto power-on by adding external pull-high resistor on the DL_KEY pin.

USB DL (auto power-on) can still be initiated by pressing DL_KEY or under valid BATON information (decided by customers' PCB options). Nonetheless, DL_KEY supports key function in normal mode. The valid BATON information can be detected through battery's NTC when it is connected to pin BATON of MT6392.

3.8 AUXADC

3.8.1 Description

The auxiliary ADC includes the following functional blocks:

- Analog multiplexer: Selects signal from one of the input channels. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
- 15-bit A/D converter: Converts the multiplexed input signal to 15-bit digital data..

Table 3-3. Application and Input Iange of ADC channels

Channel	Application	Input range [V]
0	BATSNS	2.5 ~ 4.5
1	ISENSE	2.5 ~ 4.5
2	VCDT	0 ~ 1.5
3	BATON	0.1 ~ 1.8
6	TYPE-C	0 ~ 3.3
8	DP/DM	0 ~ 3.6
others	Internal use	N/A

3.9 Fuel Gauge

The fuel gauging system includes utilizes the measurement ADC (AUXADC) for battery voltage and temperature measurement. The battery state-of-charge (SOC) estimation is performed by the software using the two measuring methods.

The principle of operation of the fuel gauge relies on a combination of Coulomb counting and light load battery voltage measurement. Coulomb counting provides an estimate of the charge that has been withdrawn or delivered to the battery, while battery voltage measurement proves a good estimate of the battery SOC under low-load conditions. The battery voltage measurement compensates for error accumulation during the current integration inherent in Coulomb counting.

3.10 Real-time Clock

The Real Time Clock (RTC) module provides time and data information. The clock is based on a 32.768kHz oscillator with an independent power supply. When the mobile handset is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor will be used. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core via the BBWAKEUP signal. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g. 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

In MT6392, RTC module also supports function without 32kHz crystal. It can be configured by hardware option. The two configurations are shown below. While crystal is absent, RTC module has an embedded 32kHz oscillator to assist life time extension after master 32kHz clock is off.

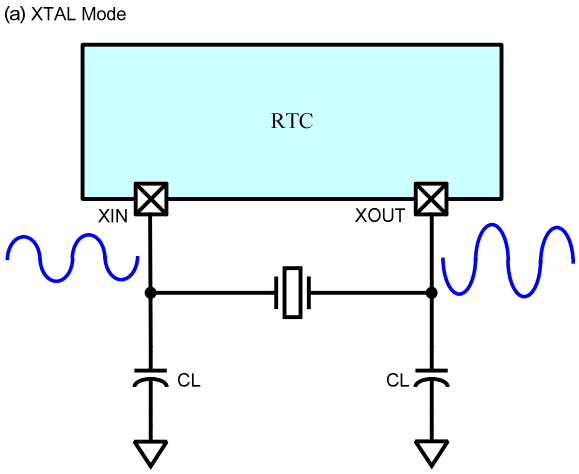


Figure 3-6. RTC configuration methods for XTAL

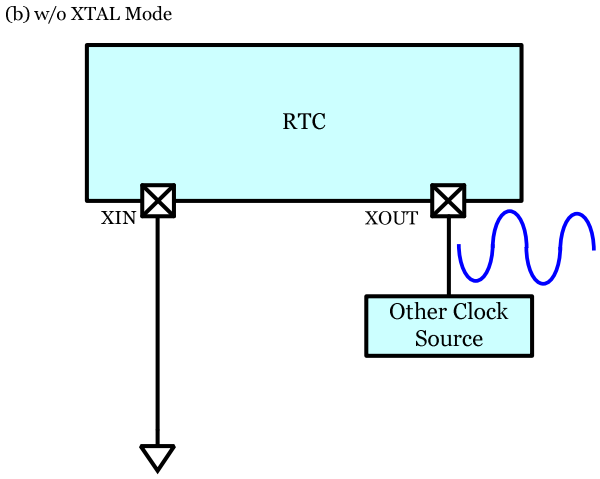


Figure 3-7. RTC configuration methods for w/o XTAL mode

3.11 32kHz Crystal Oscillator (XOSC32)

The low-power 32kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768kHz crystal and a load composed of two functional capacitors. The key performance is shown in the table below.

Table 3-4. XOSC32 functional specifications

Symbol	Parameter	Min.	Typical	Max.	Unit
VRTC	RTC module power	1.1	2.8	3.0	V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	20		80	%
I	Current consumption		5		µA
T	Operating temperature	-30		85	°C

The minimum VRTC value means if the crystal oscillator starts up successfully, the minimum VRTC for the clock to still be alive is 1.1V.

Since the crystal parameters determine the oscillation allowance, see below for a few recommendations for the crystal parameters to be used well with XOSC32 in MT6392.

Table 3-5. 32kHz crystal recommended parameters

Symbol	Parameter	Min.	Typical	Max.	Unit
F	Frequency range		32768		Hz
GL	Drive level	0.5			uW
Δf/f	Frequency tolerance		+/- 20		ppm

Symbol	Parameter	Min.	Typical	Max.	Unit
ESR	Series resistance		50	70	KΩ
C0	Static capacitance		0.9	2	pF
CL[1]	Load capacitance	6		12.5	pF

Under such CL range and crystal, the –R is greater than three times. If the CL selected is larger, the frequency accuracy will be decreased, and the –R will also degrade.

3.12 Interrupts and Watchdog

3.12.1 Interrupts

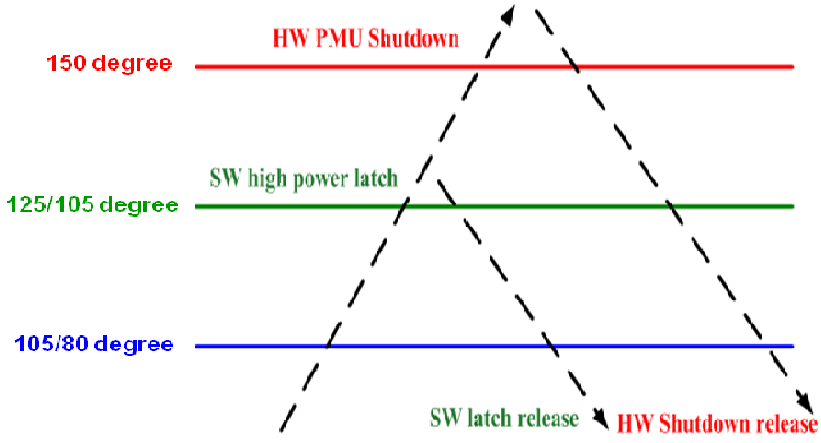
For certain dedicated events, PMIC will issue INT to AP (BB IC). The interrupt group list is as follows:

Key pressed and released interrupt

- PWRKEY: Interrupt is issued when PWRKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the PWRKEY_DEB status to see if it is pressed or released.
- FCHR_ENB: Interrupt is issued when FCHR_ENB is pressed (and released, set by the register). After receiving the interrupt, the software will read the FCHR_ENB _DEB status to see if it is pressed or released.

Thermal interrupt

- MT6392 issues THR_H interrupt for the software high power latch if PMIC die temperature is over 125°C/105°C and issues THR_L for software latch release if PMIC die temperature goes from 125°C/105°C back to under 105°C/80°C.



Charger related interrupt

- There are several interrupts supported for charger control:
  - CHRDET
  - OV
  - WATCHDOG
  - BVALID_DET
  - VBATON_UNDET

Battery voltage/current H/L interrupt

- VBAT detected by AUXADC
  If VBAT is higher than the threshold specified by an register setting, the HIGHBATTERY interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the LOWBATTERY interrupt will be issued.

Speaker OC interrupt

- MT6392 supports speaker OC interrupt generation which uses PWM detection method.

BUCK OC interrupt

- MT6392 has 3 bucks and each has its individual OC interrupt which uses PWM detection method.
  - VPROC_OC
  - VCORE_OC
  - VSYS_OC

LDO OC interrupt

- MT6392 supports LDO OC interrupt generation. It will be issued if any one of the LDOs has OC condition.

3.12.2 Watchdog Reset

WDTRSTB_IN is an input pin to receive the watchdog reset from AP. PMIC resets all modules to initial state when receiving watchdog reset from AP.

3.13 Type-C

Type-C module is used to support USB Type-C connector. Measuring CC1/CC2 (Newly added signal pins in Type-connector) voltage It can determine:

- Detect attach & detach event
- Determine orientation
- Determine power role

- Determine Source current ability

It can detect attach/detach event. Determine whether Type-C cable is plug in. Is also can determine the direction of connection when attach(cc1 or cc2). Use this information to program the correct path for USB3.0 function. Except detection, it has a close relationship with USB power Sourcing and Sinking. Must know the CC detection result before Sourcing or Sinking VBUS & VCONN. Source and Sink is DFP and USP sperately when first attach. Type-C connector also define larger current support (max 3A)then previous one.Sorce use different Rp on CC to indicate its current ability. Sink measuring voltage on CC pin to knows it. Sink must use this information to make sure its sinking current not to over port partner's ability.

Type-C module is implemented base on CC state machine in Type-C SPEC V1.1. We target to support Source, Sink, DRP & Accessory mode, so we combine each type's state machine as Figure 3-8. Sink power sub-state machine as Figure 3-9 is also implemented. Table 3-6 list each type's supporting states. It is better to know the meaning of each state which defined in SPEC and what should we do in each state before we start to use it. For example, turn on V_{BUS} after entering Attach.SRC state.

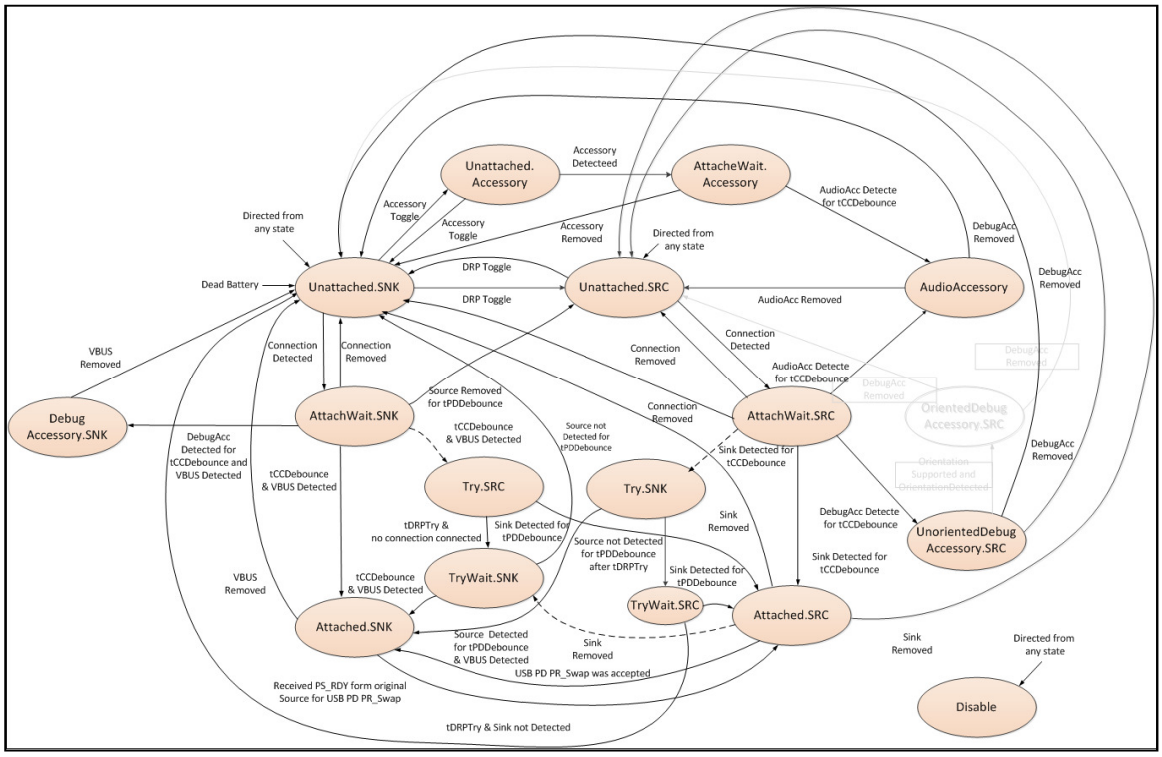


Figure 3-8. Type-C module target CC state machine

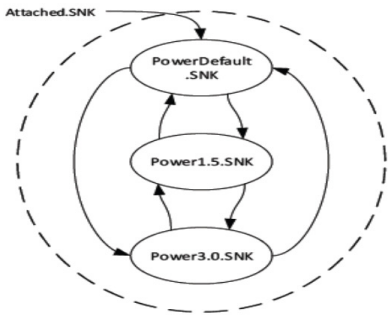


Figure 3-9. Type-C module target CC sub-power state

Table 3-6. Type-C module supported CC state

	SOURCE	SINK	DRP
Disabled	Support	Support	Support
Unattached.SNK	N/A	Support	Support
AttachWait.SNK	N/A	Support	Support
Attached.SNK	N/A	Support	Support
Unattached.SRC	Support	N/A	Support
AttachedWait.SRC	Support	N/A	Support
Attached.SRC	Support	N/A	Support
Try.SRC	N/A	N/A	Support
TryWait.SNK	N/A	N/A	Support
Try.SNK	N/A	N/A	Support
AudioAccessory	Support	Support	Support
Unattached. Accessory	N/A	Support	N/A
AttachWait.Accessory	N/A	Support	N/A
UnorientedDebugAccessory.SRC	Support	N/A	Support
DebugAccessory.SNK	N/A	Support	Support
PowerDefault.SNK	N/A	Support	Support
Power1.5.SNK	N/A	Support	Support
Power3.0.SNK	N/A	Support	Support

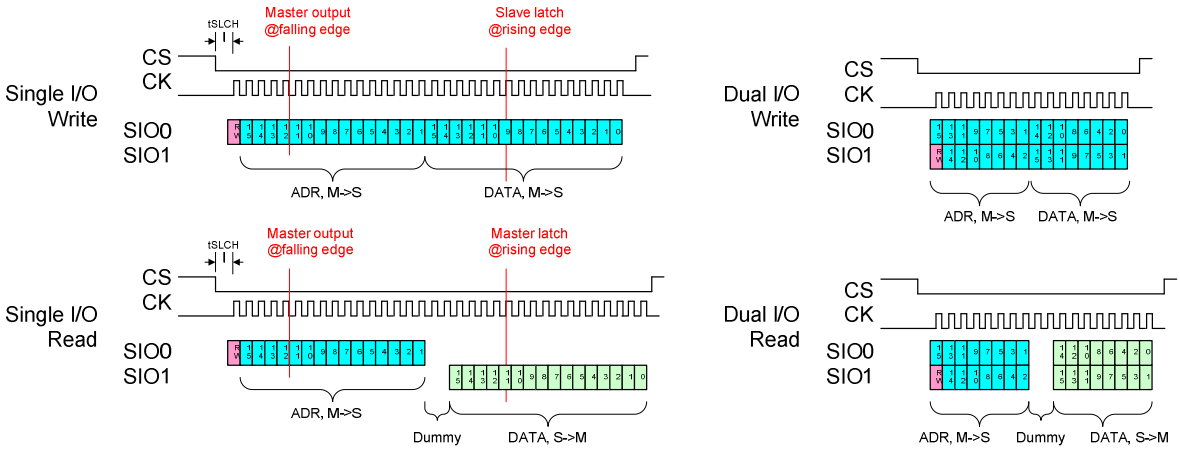
3.14 SPI Interface

PMIC uses a 4-wire interface consisting of a clock, a chip select and two data signals (MOSI and MISO) to connect to BB. This serial-parallel interface allows BB to write commands to and read status from PMIC.

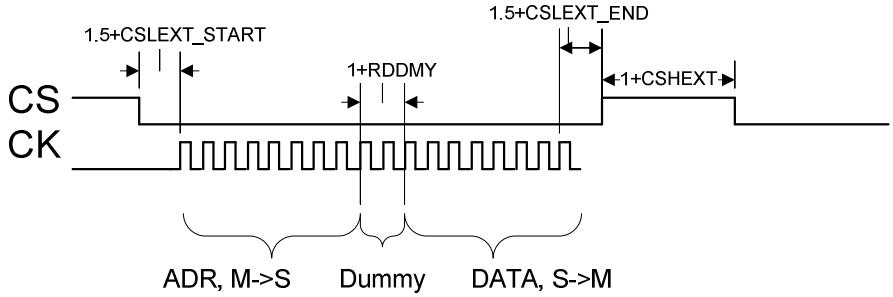
3.14.1 Data Format

The pre-defined SPI format consists of two modes: Single I/O mode and dual I/O mode. Single I/O always uses MISO as output and MOSI as input. Dual I/O uses both MOSI and MISO to be output and input to achieve better channel usage. The format conveys information of R/W direction, 1-bit R/W flag(bit 15), 15-bit address (bit 14 to bit 0) and 16-bit data, and both addresses and data are MSB first. The operation waveform of SPI is illustrated as below. The SPI slave in PMIC latch data sent from the master is at the rising edge of the clock, and output data are at the falling edge of the clock. The parameter tSLCH, tDMMY and tCHSH are fully configurable through command registers (in BB instead of PMIC) as illustrated in the figures below.

SPI format:



SPI parameter configuration:



3.15 GPIO

3.15.1 GPIO List

Table 3-7. MT6392 GPIO list

Ball Name	Aux Func.0	Aux Func.1	Aux Func.5	Aux Func.6	Aux Func.7	PU/PD
WDTRSTB_IN						
INT	GPIO0	O:INT	I0:TEST_CK2	I0:TEST_IN1	O:TEST_OUT1	UD/D
SRCLKEN	GPIO1	I1:SRCLKEN	I0:TEST_CK0	I0:TEST_IN2	O:TEST_OUT2	UD/D
RTC_32K1V8	GPIO2	O:RTC_32K1V8	I0:TEST_CK1	I0:TEST_IN3	O:TEST_OUT3	UD
SPI_CLK	GPIO3	I0:SPI_CLK				UD/D
SPI_CSN	GPIO4	I1:SPI_CSN				UD/U
SPI_MOSI	GPIO5	B0:SPI_MOSI				UD/D
SPI_MISO	GPIO6	B0:SPI_MISO		I0:TEST_IN4	O:TEST_OUT4	UD/D

3.15.2 GPIO Specification

Table 3-8. MT6392 GPIO electrical characteristics

Paramters	Descriptions	Min.	Typ.	Max.	Unit
Inputs					
VIH	Input logic low voltage	0.65*VDDQ		VDDQ+0.3	V
VIL	Input logic high voltage	-0.3		0.35*VDDQ	V
Rpu	Input pull-up resistance	40	75	190	KΩ
Rpd	Input pull-down resistance	40	75	190	KΩ
Outputs					
VOH(DC)	DC Output logic high voltage	0.75*VDDQ			V
VOL(DC)	DC Output logic low voltage			0.25*VDDQ	V

Note. VDDQ is GPIO power(VIO18).

4 Register Definitions and Descriptions

Table 4-1. Module Registers

IP name	Begin	End
PCHR (Pulse Charger)	0x0000	0x0038
STRUP (1)	0x003C	0x0050
SPK (Audio AMP)	0x0052	0x006A
STRUP (2)	0x006E	0x007E
TOP	0x0100	0x0154
INT (Interrupt)	0x0160	0x0178
FQMTR (Frequency meter)	0x0182	0x0186
SPI	0x0188	0x01A8
BUCK	0x0200	0x032E
LDO	0x0400	0x0572
EFUSE	0x0600	0x0696
RTC	0x0644	0x0646
AUXADC	0x0700	0x07B6
TYPE-C	0x0800	0x088E

Module name: PMIC_REG Base address: (+0h)

Address	Name	Width	Register Function
0000	CHR_CON0	16	Charger control register 0
0002	CHR_CON1	16	Charger Control Register 1
0004	CHR_CON2	16	Charger Control Register 2
0006	CHR_CON3	16	
0008	CHR_CON4	16	Charger Control Register 4
000C	CHR_CON6	16	Charger Control Register 6
000E	CHR_CON7	16	Charger Control Register 7
0012	CHR_CON9	16	Charger Control Register 9
0014	CHR_CON10	16	Charger Control Register 10
001A	CHR_CON13	16	Charger Control Register 13
001C	CHR_CON14	16	Charger Control Register 14
001E	CHR_CON15	16	Charger Control Register 15
0020	CHR_CON16	16	Charger Control Register 16
0024	CHR_CON18	16	
0026	CHR_CON19	16	Charger Control Register 19
0028	CHR_CON20	16	Charger Control Register 20
002A	CHR_CON21	16	Charger Control Register 21
002C	CHR_CON22	16	

Module name: PMIC_REG Base address: (+0h)

002E	CHR_CON23	16	Charger Control Register 23
0036	CHR_CON27	16	
0038	CHR_CON28	16	Charger Control Register 28
003A	CHR_CON29	16	Charger Control Register 29
003C	STRUP_CON0	16	STRUP control register 0
0040	STRUP_CON3	16	STRUP control register 3
0044	STRUP_CON5	16	STRUP control register 5
004A	STRUP_CON8	16	STRUP control register 8
004E	STRUP_CON10	16	STRUP control register 10
0052	SPK_CON0	16	Speaker Control Register 0
0056	SPK_CON2	16	Speaker Control Register 2
005E	SPK_CON6	16	Speaker Control Register 6
0062	SPK_CON8	16	Speaker Control Register 8
0064	SPK_CON9	16	Speaker Control Register 9
006A	SPK_CON12	16	Speaker Control Register 12
0070	STRUP_CON13	16	STRUP control register 13
0078	STRUP_CON17	16	STRUP control register 17
007A	STRUP_CON18	16	STRUP control register 18
007C	STRUP_CON19	16	STRUP control register 19
011A	TOP_RST_MISC	16	reset control misc
0142	CHRSTATUS	16	CHR Status
0144	TDSEL_CON	16	TDSEL_CON
0146	RDSEL_CON	16	RDSEL_CON
0148	SMT_CON0	16	SMT_CON0
014A	SMT_CON1	16	SMT_CON1
0152	DRV_CON0	16	DRV_CON0
0154	DRV_CON1	16	DRV_CON1
0182	FQMTR_CON0	16	Frequency meter control register 0
0184	FQMTR_CON1	16	Frequency meter control register 1
0186	FQMTR_CON2	16	Frequency meter control register 2
0210	VPROC_CON2	16	VPROC control register 2
0212	VPROC_CON3	16	VPROC control register 3
021A	VPROC_CON7	16	VPROC control register 7
021E	VPROC_CON9	16	VPROC control register 9
0220	VPROC_CON10	16	VPROC control register 10
0222	VPROC_CON1	16	VPROC control register 11

Module name: PMIC_REG Base address: (+0h)

	1		
0224	VPROC_CON12	16	VPROC control register 12
0236	VSYS_CON2	16	VSYS control register 2
0240	VSYS_CON7	16	VSYS control register 7
0244	VSYS_CON9	16	VSYS control register 9
0246	VSYS_CON10	16	VSYS control register 10
0248	VSYS_CON11	16	VSYS control register 11
024A	VSYS_CON12	16	VSYS control register 12
0258	BUCK_OC_CON0	16	BUCK_OC control register 0
025E	BUCK_OC_CON3	16	BUCK_OC control register 3
0260	BUCK_OC_CON4	16	BUCK_OC control register 4
0304	VCORE_CON2	16	VCORE control register 2
0306	VCORE_CON3	16	VCORE control register 3
030E	VCORE_CON7	16	VCORE control register 7
0312	VCORE_CON9	16	VCORE control register 9
0314	VCORE_CON10	16	VCORE control register 10
0316	VCORE_CON11	16	VCORE control register 11
0318	VCORE_CON12	16	VCORE control register 12
0402	ANALDO_CON1	16	Analog LDO control register 1
0404	ANALDO_CON2	16	Analog LDO control register 2
0408	ANALDO_CON4	16	Analog LDO control register 4
0412	ANALDO_CON10	16	Analog LDO control register 10
0420	ANALDO_CON21	16	Analog LDO control register 21
0424	ANALDO_CON23	16	Analog LDO control register 23
0428	ANALDO_CON25	16	Analog LDO control register 25
042E	ANALDO_CON28	16	Analog LDO control register 28
0500	DIGLDO_CON0	16	Digital LDO control register 0
0502	DIGLDO_CON2	16	Digital LDO control register 2
0504	DIGLDO_CON3	16	Digital LDO control register 3
0506	DIGLDO_CON5	16	Digital LDO control register 5

Module name: PMIC_REG Base address: (+0h)

0508	DIGLDO_CON6	16	Digital LDO control register 6
050A	DIGLDO_CON7	16	Digital LDO control register 7
050C	DIGLDO_CON8	16	Digital LDO control register 8
0512	DIGLDO_CON11	16	Digital LDO control register 11
051A	DIGLDO_CON15	16	Digital LDO control register 15
052A	DIGLDO_CON24	16	Digital LDO control register 24
052C	DIGLDO_CON26	16	Digital LDO control register 26
0530	DIGLDO_CON28	16	Digital LDO control register 28
0532	DIGLDO_CON29	16	Digital LDO control register 29
0536	DIGLDO_CON31	16	Digital LDO control register 31
0538	DIGLDO_CON32	16	Digital LDO control register 32
0552	DIGLDO_CON47	16	Digital LDO control register 47
0556	DIGLDO_CON49	16	Digital LDO control register 49
055A	DIGLDO_CON51	16	Digital LDO control register 51
055C	DIGLDO_CON52	16	Digital LDO control register 52
055E	DIGLDO_CON53	16	Digital LDO control register 53
0562	DIGLDO_CON55	16	Digital LDO control register 55
0566	DIGLDO_CON57	16	Digital LDO control register 57
0570	DIGLDO_CON62	16	Digital LDO control register 62
0700	AUXADC_ADC0	16	AUXADC ADC register 0
0702	AUXADC_ADC1	16	AUXADC ADC register 1
0704	AUXADC_ADC2	16	AUXADC ADC register 2
0706	AUXADC_ADC3	16	AUXADC ADC register 3
0708	AUXADC_ADC4	16	AUXADC ADC register 4
070A	AUXADC_ADC5	16	AUXADC ADC register 5
070C	AUXADC_ADC6	16	AUXADC ADC register 6
070E	AUXADC_ADC7	16	AUXADC ADC register 7

Module name: PMIC_REG Base address: (+0h)

0710	AUXADC_ADC8	16	AUXADC ADC register 8
0712	AUXADC_ADC9	16	AUXADC ADC register 9
0714	AUXADC_ADC10	16	AUXADC ADC register 10
0716	AUXADC_ADC11	16	AUXADC ADC register 11
0718	AUXADC_ADC12	16	AUXADC ADC register 12
071A	AUXADC_ADC13	16	AUXADC ADC register 13
071C	AUXADC_ADC14	16	AUXADC ADC register 14
071E	AUXADC_ADC15	16	AUXADC ADC register 15
0720	AUXADC_ADC16	16	AUXADC ADC register 16
0726	AUXADC_ADC19	16	AUXADC ADC register 19
072A	AUXADC_ADC21	16	AUXADC ADC register 21
072C	AUXADC_ADC22	16	AUXADC ADC register 22
072E	AUXADC_STA0	16	AUXADC_STA0
0730	AUXADC_STA1	16	AUXADC_STA1
0800	TYPE_C_PHY_RG_0	16	TYPE-C PHY RG 0
0806	TYPE_C_CTRL	16	TYPE-C Control
080A	TYPE_C_CC_SW_CTRL	16	TYPE-C CC Stoftware Control
080C	TYPE_C_CC_VOL_PERIODIC_MEAS_VAL	16	TYPE-C CC Voltage Periodic Measure Value
080E	TYPE_C_CC_VOL_DEBOUCE_CNT_VAL	16	TYPE-C CC Voltage Debounce Count Value
0810	TYPE_C_DRP_SRC_CNT_VAL_0	16	TYPE-C DRP Source Count Value 0
0814	TYPE_C_DRP_SNK_CNT_VAL_0	16	TYPE-C DRP Sink Count Value 0
0818	TYPE_C_DRP_TRY_CNT_VAL_0	16	TYPE-C DRP Try Count Value 0
0820	TYPE_C_CC_SRC_DEFAULT_DAC_VAL	16	TYPE-C CC SRC Default DAC Value
0822	TYPE_C_CC_SRC_15_DAC	16	TYPE-C CC SRC 15 DAC Value

Module name: PMIC_REG Base address: (+0h)

	VAL		
0824	TYPE_C_CC_SRC_30_DAC_VAL	16	TYPE-C CC SRC 30 DAC Value
0828	TYPE_C_CC_SNK_DAC_VAL_0	16	TYPE-C CC SNK DAC Value 0
082A	TYPE_C_CC_SNK_DAC_VAL_1	16	TYPE-C CC SNK DAC Value 1
0830	TYPE_C_INTR_EN_0	16	TYPE-C Interrupt Enable 0
0834	TYPE_C_INTR_EN_2	16	TYPE-C Interrupt Enable 2
0838	TYPE_C_INTR_0	16	TYPE-C Interrupt 0
083C	TYPE_C_INTR_2	16	TYPE-C Interrupt 2
0840	TYPE_C_CC_STATUS	16	TYPE-C CC Status
0842	TYPE_C_PWR_STATUS	16	TYPE-C Power Status

0000 CHR_CON0 Charger control register 0 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RGS_VCDT_HV_DET	RGS_VCDT_LV_DET	RGS_CHRDET	RG_CHR_EN	RG_CSDAC_EN		RGS_CHR_LDO_DET	RG_VCDT_HV_EN
Type									RO	RO	RO	RW	RW		RO	RW
Reset									0	0	0	0	0		0	1

Bit(s)	Mnemonic	Name	Description
7	RGS_VCDT_HV_DET	RGS_VCDT_HV_DET	**ChargerIn threshould detection (1: > vth, 0 < vth), vth is according to RG_VCDT_HV_VTH[3:0] and RG_VCDT_LV_VTH[3:0] setting** 0000~0001: 4.0, 4.1 with 100mV/step 0010~1000: 4.15V~4.45V with 50mV/step 1001~1100: 6V~7.5V with 500mV/step 1101~1111: 8.5V~10.5V with 1000mV/step
6	RGS_VCDT_LV_DET	RGS_VCDT_LV_DET	**ChargerIn threshould detection (1: > vth, 0 < vth), vth is according to RG_VCDT_HV_VTH[3:0] and RG_VCDT_LV_VTH[3:0] setting** 0000~0001: 4.0, 4.1 with 100mV/step 0010~1000: 4.15V~4.45V with 50mV/step 1001~1100: 6V~7.5V with 500mV/step 1101~1111: 8.5V~10.5V with 1000mV/step
5	RGS_CHRDET	RGS_CHRDET	**Charger-in detect.** 0: No valid charger detected

Bit(s)	Mnemonic	Name	Description
			1: Valid charger detected
4	**RG_CHR_EN**	RG_CHR_EN	**Charger enable setting, which would gated CSDAC_EN, PCHR_AUTO and HWCV_EN** 0: Charger disabled 1: Charger enabled
3	**RG_CSDAC_EN**	RG_CSDAC_EN	**CS DAC enable.** 0: CS DAC disabled 1: CS DAC enabled
1	**RGS_CHR_LDO_DET**	RGS_CHR_LDO_DET	**Charger LDO detection. If not detected, pulse charger cannot work.** 0: Invalid charger LDO (<2.35v) 1: Valid charger LDO (>2.52v)
0	**RG_VCDT_HV_EN**	RG_VCDT_HV_EN	**Charger-in high voltage detection comparator enable.** 0: disable. Only compare LV threshold 1: enable. Compare both LV and HV threshold

0002 **CHR_CON1** **Charger Control Register 1** **00F5**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VCDT_HV_VTH				RG_VCDT_LV_VTH			
Type									RW				RW			
Reset									1	1	1	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description
7:4	**RG_VCDT_HV_VTH**	RG_VCDT_HV_VTH	**ChargerIn LV detection threshold, default 4.3/10.5V for VTHL/VTHH** 0000~0001: 4.0, 4.1 with 100mV/step 0010~1000: 4.15V~4.45V with 50mV/step 1001~1100: 6V~7.5V with 500mV/step 1101~1111: 8.5V~10.5V with 1000mV/step
3:0	**RG_VCDT_LV_VTH**	RG_VCDT_LV_VTH	**ChargerIn LV detection threshold, default 4.3/10.5V for VTHL/VTHH** 0000~0001: 4.0, 4.1 with 100mV/step 0010~1000: 4.15V~4.45V with 50mV/step 1001~1100: 6V~7.5V with 500mV/step 1101~1111: 8.5V~10.5V with 1000mV/step

0004 **CHR_CON2** **Charger Control Register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RGS_VBAT_CC_DET	RGS_VBAT_CV_DET	RGS_CS_DET		RG_CS_EN		RG_VBAT_CV_EN	
Type									RO	RO	RO		RW		RW	
Reset									0	0	0		0		0	

Bit(s)	Mnemonic	Name	Description
7	**RGS_VBAT_CC_DET**	RGS_VBAT_CC_DET	**VBAT voltage detection for CC.** 0: VBAT voltage < VBAT_CC_VTH 1: VBAT voltage > VBAT_CC_VTH
6	**RGS_VBAT_CV_DET**	RGS_VBAT_CV_DET	**VBAT voltage detection for CV.** 0: VBAT voltage < VBAT_CV_VTH 1: VBAT voltage > VBAT_CV_VTH
5	**RGS_CS_DET**	RGS_CS_DET	**Current sense voltage detection.** 0: CS voltage < CS_VTH 1: CS voltage > CS_VTH
3	**RG_CS_EN**	RG_CS_EN	**Current sense voltage detection comparator enable.** 0: Disabled 1: Enabled
1	**RG_VBAT_CV_EN**	RG_VBAT_CV_EN	**Battery CV detection enable** 0: Disabled 1: Enabled

0006 **CHR_CON3** **000D**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_VBAT_CV_VTH				
Type												RW				
Reset												0	1	1	0	1

Bit(s)	Mnemonic	Name	Description
4:0	**RG_VBAT_CV_VTH**	RG_VBAT_CV_VTH	**Battery CV dection threshold trimming option, default 4.2V** this register is used for FT CV threshold trimming and not for customer's fine tuning (pchr_dig should invert MSB bit. otherwise, BC1.1 2.2V threshold would be wrong) MT6392 rearrange CV mapping, pchr_dig should revise to follow the new mapping. 00000 -> 00011: 3.775, 3.800, 3.850, 3.900 00100 -> 00111: 4.000, 4.050, 4.100, 4.125 01000 -> 01011: 4.1375, 4.150, 4.1625, 4.175 01100 -> 01111: 4.1875, 4.200, 4.2125, 4.225 10000 -> 10011: 4.2375, 4.25, 4.2625, 4.275 10100 -> 10111: 4.2875, 4.3, 4.3125, 4.325 11000 -> 11001: 4.3375, 4.35,4.3625,4.375 11010 -> 11110: 4.3875,4.4,4.425 11111: 2.2V (used in BC1.1 application)

0008 **CHR_CON4** **Charger Control Register 4** **000F**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_CS_VTH			
Type													RW			
Reset													1	1	1	1

Bit(s)	Mnemonic	Name	Description
			Current sense voltage detection threshold @ Rcs=0.20hm
3:0	**RG_CS_VTH**	RG_CS_VTH	0: 1600mA 1: 1500mA 2: 1400mA 3: 1300mA 4: 1200mA 5: 1100mA 6: 1000mA 7: 900mA 8: 800mA 9: 700mA 10: 650mA 11: 550mA 12: 450mA (USB download) 13: 300mA 14: 200mA 15: 70mA

000C **CHR_CON6** **Charger Control Register 6** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VBAT_OV_DET	RG_VBAT_OV_DEG		RG_VBAT_OV_VTH			RG_VBAT_OV_EN
Type										RO	RW		RW			RW
Reset										0	0		0	0	0	1

Bit(s)	Mnemonic	Name	Description
6	**VBAT_OV_DET**	RGS_VBAT_OV_DET	**VBAT_OV voltage detection.** 0 VBAT voltage < VBAT_OV_VTH 1 VBAT voltage > VBAT_OV_VTH
5	**RG_VBAT_OV_DEG**	RG_VBAT_OV_DEG	**VBAT OV voltage detection deglitch enable.** 0 no debounce 1 debounce one cycle (1us)
3:1	**RG_VBAT_OV_VTH**	RG_VBAT_OV_VTH	**Battery over-voltag detection threshold** 000: 4.200V (default) 001: 4.300V 010: 4.400V 011: 4.450V 1xx: 3.800V
0	**RG_VBAT_OV_EN**	RG_VBAT_OV_EN	**VBAT OV over-voltage detection comparator enable.**

000E **CHR_CON7** **Charger Control Register 7** **0001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

000E **CHR_CON7** **Charger Control Register 7** **0001**

Name				RGS_BATON_UNDET										BATON_TDET_EN	RG_BATON_HT_EN	RG_BATON_EN
Type				RO										RW	RW	RW
Reset				0										0	0	1

Bit(s)	Mnemonic	Name	Description
12	RGS_BATON_UNDET	RGS_BATON_UNDET	**BATON_UNDET voltage detection. BATON_UNDET always is 0 during DDLO/UVLO** 0: Valid battery detected 1: Valid battery not detected
2	BATON_TDET_EN	BATON_TDET_EN	**0: N/A** 1: Enable BATON Temperature detection
1	RG_BATON_HT_EN	RG_BATON_HT_EN	**Battery-On HW high temperature detection** 0: Disabled 1: Enabled, RG_BATON_EN must be 1
0	RG_BATON_EN	RG_BATON_EN	**BATON_UNDET detection enable.** 0: Comparator disabled and BATON_UNDET = 0 1: Compare enabled

0012 **CHR_CON9** **Charger Control Register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_FRC_CSVTH_USBDL
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0	RG_FRC_CSVTH_USBDL	RG_FRC_CSVTH_USBDL	**Force CS DAC detection threshold to maximum in USB download mode** 0: CS_VTH=450mA in USBDL mode 1: CS_VTH=1600mA in USBDL mode

0014 **CHR_CON10** **Charger Control Register 10** **0020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Nam										RG	RG					

0014 CHR_CON10 Charger Control Register 10 0020

Name										S_OTG_BVALID_DET	_OTG_BVALID_EN					
Type										RO	RW					
Reset										0	1					

Bit(s)	Mnemonic	Name	Description
6	RGS_OTG_BVALID_DET	RGS_OTG_BVALID_DET	**Indicates if the session for B-peripheral is valid (0.8V<Vth<4V). Here VBUS is connected to CHRIN.** 0: Vbus < 0.8V 1: Vbus > 4V, RG_OTG_BVALID_EN must be 1
5	RG_OTG_BVALID_EN	RG_OTG_BVALID_EN	**BVALID detect enable.** 0: Disabled 1: Enabled

001A CHR_CON13 Charger Control Register 13 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_CHRWDT_WR				RG_CHRWDT_EN	RG_CHRWDT_TD			
Type								RW				RW	RW			
Reset								0				1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8	RG_CHRWDT_WR	RG_CHRWDT_WR	**To reset charger watch-dog timer and update CHRWDT_TD** 0: reset inactive 1: reset active and CHRWDT_TD updated to PCHR_DIG
4	RG_CHRWDT_EN	RG_CHRWDT_EN	**Enable setting for charger watch-dog timer** 0: Disabled 1: Enabled if (CHR_EN(@CHR_CON0) == 1) Note1: UVLO don't care this bit and will timeout after 3000s Note2: PCHR_TESTMODE can force to control watch-dog enable by using this bit
3:0	RG_CHRWDT_TD	RG_CHRWDT_TD	**Time constant setting for charger watch-dog timer** 0: 4 sec 1: 8 sec 2: 16 sec 3: 32 sec 4: 128 sec 5: 256 sec 6: 512 sec 7: 1024 sec 8~15: 3000 sec

001C **CHR_CON14** **Charger Control Register 14** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_PCHR_RV							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	RG_PCHR_RV	RG_PCHR_RV	Reserved for testing

001E **CHR_CON15** **Charger Control Register 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RGS_CHRWDT_OUT	RG_CHRWDT_FLAG_WR	RG_CHRWDT_INT_EN
Type														RO	RW	RW
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	RGS_CHRWDT_OUT	RGS_CHRWDT_OUT	**Time-out flag for charger watch-dog timer** Read: 0: No time-out status 1: Time-out status asserted
1	RG_CHRWDT_FLAG_WR	RG_CHRWDT_FLAG_WR	**Clear time-out flag for charger watch-dog timer** Read: 0: N/A (while RGS_CHRWDT_OUT=0) 1: Clear time-out flag while RGS_CHRWDT_OUT=1
0	RG_CHRWDT_INT_EN	RG_CHRWDT_INT_EN	**Interrupt enable setting for charger watch-dog timer.** 0: Disabled 1: Enabled

0020 **CHR_CON16** **Charger Control Register 16** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				ADCIN_VCHR_EN	ADCIN_VSEN_EN	ADCIN_VBAT_EN	RG_ADCIN_VSEN_EX	ADCIN_VSEN_MUX_E					RG_USBDL_SET	RG_USBDL_RST	RG_UVLO_VTHL	

0020 CHR_CON16 Charger Control Register 16 0000

							T_BATON_EN	N								
Type				RW	RW	RW	RW	RW					RW	RW	RW	
Reset				0	0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
12	ADCIN_VCHR_EN	ADCIN_VCHR_EN	**AUXADC input source enable for VCHR.** 0: Disabled 1: Enabled
11	ADCIN_VSEN_EN	ADCIN_VSEN_EN	**AUXADC input source enable for VSEN.** 0: Disabled 1: Enabled
10	ADCIN_VBAT_EN	ADCIN_VBAT_EN	**AUXADC input source enable for VBAT.** 0: Disabled 1: Enabled
9	RG_ADCIN_VSEN_EXT_BATON_EN	RG_ADCIN_VSEN_EXT_BATON_EN	**0: Disabled** 1: Enabled
8	ADCIN_VSEN_MUX_EN	ADCIN_VSEN_MUX_EN	**AUXADC input source enable for VSEN to be switched to VBAT's divider** 0: Disabled 1: Enabled
3	RG_USBDL_SET	RG_USBDL_SET	**USBDL_MODE software set control** 0: No effect 1: Force enter USBDL MODE
2	RG_USBDL_RST	RG_USBDL_RST	**USBDL_MODE software reset control** 0: No effect 1: Force leave USBDL MODE (priority is less than USBDL_DET)
1:0	RG_UVLO_VTHL	RG_UVLO_VTHL	**UVLO low threshold selection** 00: 2.9V (default) 01: 2.75V 10: 2.6V 11: 2.5V

0024 CHR_CON18 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_BUF_DM_IN_EN	RG_BUF_DP_IN_EN	RG_DPDM_ADCBUF_EN	RG_DPDM_ADCSW_EN	RGS_BC11_CMP_OUT				RG_BC11_VSRC_EN		RG_BC11_RST	RG_BC11_BB_CTRL
Type					RW	RW	RW	RW	RO				RW		RW	RW
Reset					0	0	0	0	0				0	0	0	0

Bit(s)	Mnemonic	Name	Description
11	**RG_BUF_DM_IN_EN**	RG_BUF_DM_IN_EN	**charging port detection DP/DM buffer** buffer input of PAD_CHG_DM enable 1: enable 0: disable
10	**RG_BUF_DP_IN_EN**	RG_BUF_DP_IN_EN	**charging port detection DP/DM buffer** buffer input of PAD_CHG_DP enable 1: enable 0: disable
9	**RG_DPDM_ADCBUF_EN**	RG_DPDM_ADCBUF_EN	**charging port detection DP/DM buffer** buffer enable 1: enable 0: disable
8	**RG_DPDM_ADCSW_EN**	RG_DPDM_ADCSW_EN	**charging port detection DP/DM buffer** output SW for AUXADC 1: enable 0: disable
7	**RGS_BC11_CMP_OUT**	RGS_BC11_CMP_OUT	**Comparison result of BC11 charger detection** 0: DP or DM < BC11_VREF_VTH 1: DP or DM > BC11_VREF_VTH
3:2	**RG_BC11_VSRC_EN**	RG_BC11_VSRC_EN	**BC11 voltage source. Set VDP_SRC = 0.6V** 0: disable the voltage 1: enable the voltage source to DM 2: enable the voltage source to DP 3: forbidden
1	**RG_BC11_RST**	RG_BC11_RST	**Reset BC11 detection mechanism in PCHR_DIG** 0: No effect 1: BC11 detection mechanism is disabled in PCHR_DIG, (reset timer)
0	**RG_BC11_BB_CTRL**	RG_BC11_BB_CTRL	**Force BC11 charger detection controlled by baseband** 0: BC11 detection by PCHR_DIG (hardware mode) 1: BC11 detection by baseband (software mode)

0026 **CHR_CON19** **Charger Control Register 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**RG_BC11_BIAS_EN**	**RG_BC11_IPU_EN**		**RG_BC11_IPD_EN**		**RG_BC11_CMP_EN**		**RG_BC11_VREF_VTH**	
Type								RW	RW		RW		RW		RW	
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8	**RG_BC11_BIAS_EN**	RG_BC11_BIAS_EN	**Enable BC11 detection bias circuit** 0: Disabled 1: Enabled
7:6	**RG_BC11**	RG_BC11_IPU_E	**BC11 7~15uA pull up current enable**

Bit(s)	Mnemonic	Name	Description
	_IPU_EN	N	0: disable the pull-up current 1: enable the pull-up current to DM 2: enable the pull-up current to DP 3: forbidden
5:4	**RG_BC11_IPD_EN**	RG_BC11_IPD_EN	**BC11 50~150uA pull down current** 0: disable the pull-down current 1: enable the pull-down current to DM 2: enable the pull-down current to DP 3: forbidden
3:2	**RG_BC11_CMP_EN**	RG_BC11_CMP_EN	**BC11 comparator connection** 0: disable the comparator 1: enable the comparator to DM 2: enable the comparator to DP 3: forbidden
0	**RG_BC11_VREF_VTH**	RG_BC11_VREF_VTH	**VREF threshold voltage for comparator** 0: VREF_VTH=0.325V 1: VREF_VTH=1.2V

0028 **CHR_CON20** **Charger Control Register 20** **0022**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_CSDAC_STP_DEC				RG_CSDAC_STP_INC		
Type										RW				RW		
Reset										0	1	0		0	1	0

Bit(s)	Mnemonic	Name	Description
6:4	**RG_CSDAC_STP_DEC**	RG_CSDAC_STP_DEC	**CS DAC step size for soft-start control. (tracking Decrease)** 0: step = 1 (add 1 DAC code after CSDAC_DLY delay time) 1: step = 1 (add 1 DAC code after CSDAC_DLY delay time) 2: step = 2 (add 2 DAC code after CSDAC_DLY delay time) 3: step = 3 (add 3 DAC code after CSDAC_DLY delay time) 4: step = 4 (add 4 DAC code after CSDAC_DLY delay time) 5: step = 5 (add 5 DAC code after CSDAC_DLY delay time) 6: step = 6 (add 6 DAC code after CSDAC_DLY delay time) 7: step = 7 (add 7 DAC code after CSDAC_DLY delay time)
2:0	**RG_CSDAC_STP_INC**	RG_CSDAC_STP_INC	**CS DAC step size for soft-start control. (tracking increase)** 0: step = 1 (add 1 DAC code after CSDAC_DLY delay time) 1: step = 1 (add 1 DAC code after CSDAC_DLY delay time) 2: step = 2 (add 2 DAC code after CSDAC_DLY delay time) 3: step = 3 (add 3 DAC code after CSDAC_DLY delay time) 4: step = 4 (add 4 DAC code after CSDAC_DLY delay time) 5: step = 5 (add 5 DAC code after CSDAC_DLY delay time) 6: step = 6 (add 6 DAC code after CSDAC_DLY delay time) 7: step = 7 (add 7 DAC code after CSDAC_DLY delay time)

002A **CHR_CON21** **Charger Control Register 21** **0024**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_CSDAC_STP				RG_CSDAC_DLY		

002A **CHR_CON21** **Charger Control Register 21** **0024**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Type										RW				RW		
Reset										0	1	0		1	0	0

Bit(s)	Mnemonic	Name	Description
6:4	RG_CSDAC_STP	RG_CSDAC_STP	**CS DAC step size for soft-start control.** 0: step = 1 (add 1 DAC code after CSDAC_DLY delay time) 1: step = 1 (add 1 DAC code after CSDAC_DLY delay time) 2: step = 2 (add 2 DAC code after CSDAC_DLY delay time) 3: step = 3 (add 3 DAC code after CSDAC_DLY delay time) 4: step = 4 (add 4 DAC code after CSDAC_DLY delay time) 5: step = 5 (add 5 DAC code after CSDAC_DLY delay time) 6: step = 6 (add 6 DAC code after CSDAC_DLY delay time) 7: step = 7 (add 7 DAC code after CSDAC_DLY delay time)
2:0	RG_CSDAC_DLY	RG_CSDAC_DLY	**CS DAC delay time of each step for soft-start control.** 0: 16 uS 1: 32 uS 2: 64 uS 3: 128 uS 4: 256 uS 5: 512 uS 6: 1024 uS 7: 2048 uS

002C **CHR_CON22** **0004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_LOW_ICH_DB					
Type											RW					
Reset											0	0	0	1	0	0

Bit(s)	Mnemonic	Name	Description
5:0	RG_LOW_ICH_DB	RG_LOW_ICH_DB	**Plug out HW detection debounce time (base=16ms).** Debounce time: RG_LOW_ICH_DB x 16ms

002E **CHR_CON23** **Charger Control Register 23** **0010**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_ULC_DET_EN	RG_HWCV_EN		RG_TRACKING_EN		RG_CSDAC_MODE	RG_VCDT_MODE	RG_CV_MODE
Type									RW	RW		RW		RW	RW	RW
Reset									0	0		1		0	0	0

Bit(s)	Mnemonic	Name	Description
7	**RG_ULC_DET_EN**	RG_ULC_DET_EN	**Enable charger plug out auto detection. This fuction has to be applied with RG_HWCV_EN=1.** 0: Disabled 1: Enabled
6	**RG_HWCV_EN**	RG_HWCV_EN	**Enable hardware CV current tracking** 0: Disabled 1: Enabled
4	**RG_TRACKING_EN**	RG_TRACKING_EN	**1: Enable HTH / LTH for current tracking** 0: N/A 1: Enabled
2	**RG_CSDAC_MODE**	RG_CSDAC_MODE	**0: If not entering CC, charging is AUTO mode** 1: If leaving UVLO, charging is controlled by RG_CSDAC_EN (same as CC mode)
1	**RG_VCDT_MODE**	RG_VCDT_MODE	**Charger detection mode selection** 0: Charger detection can only be active in off state 1: Charger detection is active in both on and off state
0	**RG_CV_MODE**	RG_CV_MODE	**Battery CV detection mode selection.** 0: CV detection can only be active in off state 1: CV detection is active in both on and off state

0036 **CHR_CON27** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											QI_BGR_EXT_BUF_EN					
Type											RW					
Reset											0					

Bit(s)	Mnemonic	Name	Description
5	**QI_BGR_EXT_BUF_EN**	QI_BGR_EXT_BUF_EN	**Bandgap reference buffer for external ussage (MT8320)**

0038 **CHR_CON28** **Charger Control Register 28** **0055**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_DAC_USBDL_MAX									
Type							RW									
Reset							0	0	0	1	0	1	0	1	0	1

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
9:0	**RG_DAC_USBDL_MAX**	RG_DAC_USBDL_MAX	**CS DAC maximum limit. When under USB download mode, CS DAC valuse is limited by this setting (default=450mA)**

003A CHR_CON29 Charger Control Register 29 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_PCHR_RSV							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**RG_PCHR_RSV**	RG_PCHR_RSV	**Reserved**

003C STRUP_CON0 STRUP control register 0 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											THR_HWPDN_EN					
Type											RW					
Reset											0					

Bit(s)	Mnemonic	Name	Description
5	**THR_HWPDN_EN**	THR_HWPDN_EN	**Thermal auto power down partial high current driver HW enable** (for stage 2 : 125/105 degreeC)

0040 STRUP_CON3 STRUP control register 3 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														RG_FCHR_PU_EN	RG_FCHR_KEYDET_EN	
Type														RW	RW	
Reset														0	0	

Bit(s)	Mnemonic	Name	Description
2	**RG_FCHR_PU_EN**	RG_FCHR_PU_EN	**FCHR internal resistor pull up enable** 0: disable pull up R 1: enable pull up R ==> normal key function
1	**RG_FCHR_KEYDET_EN**	RG_FCHR_KEYDET_EN	**FCHR mode state hold without key press detection feature** 1 disable 0 enable

0044 **STRUP_CON5** **STRUP control register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						PMU_THR_STATUS										
Type						RO										
Reset						0	0	0								

Bit(s)	Mnemonic	Name	Description
10:8	**PMU_THR_STATUS**	PMU_THR_STATUS	**Thermal detection status** 000: below 105/80 degreeC 001: 105/80 ~ 125/105 degreeC 011: 125/105~150 degreeC 111: 150 degreeC

004A **STRUP_CON8** **STRUP control register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QI_OSC_EN	JUST_PWRKEY_RST														
Type	RO	RO														
Reset	0	0														

Bit(s)	Mnemonic	Name	Description
15	**QI_OSC_EN**	QI_OSC_EN	**Internal oscillaotr enable**
14	**JUST_PWRKEY_RST**	JUST_PWRKEY_RST	**Long pressed reset indicator**

004E **STRUP_CON10** **STRUP control register 10** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									STRUP_AUXADC_RSTB_SEL	STRUP_AUXADC_START_SEL	STRUP_AUXADC_RSTB_SW	STRUP_AUXADC_START_SW				
Type									RW	RW	RW	RW				
Reset									0	0	0	0				

Bit(s)	Mnemonic	Name	Description
7	**STRUP_AUXADC_RSTB_SEL**	STRUP_AUXADC_RSTB_SEL	**STRUP_AUXADC_RSTB selection** 0 : HW control 1 : SW control
6	**STRUP_AUXADC_START_SEL**	STRUP_AUXADC_START_SEL	**STRUP_AUXADC_START selection** 0 : HW control 1 : SW control
5	**STRUP_AUXADC_RSTB_SW**	STRUP_AUXADC_RSTB_SW	**STRUP_AUXADC_RSTB SW path**
4	**STRUP_AUXADC_START_SW**	STRUP_AUXADC_START_SW	**STRUP_AUXADC_START SW path**

0052 **SPK_CON0** **Speaker Control Register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SPK_THER_SHDN_L_EN	SPK_OC_SHDN_DL						SPKMODE_L		SPK_EN_L
Type							RW	RW						RW		RW
Reset							0	0						0		0

Bit(s)	Mnemonic	Name	Description
9	**SPK_THER_SHDN_L_EN**	SPK_THER_SHDN_L_EN	**Speaker L-ch thermal shut down enable** **0: disable 1: enable**
8	**SPK_OC**	SPK_OC_SHDN	**class D mode L-ch OC event shutdown**

Bit(s)	Mnemonic	Name	Description
	_SHDN_DL	_DL	**0: disable 1: enable**
2	**SPKMODE_L**	SPKMODE_L	**speaker L-ch driver mode select** **0: class D mode 1: class AB mode**
0	**SPK_EN_L**	SPK_EN_L	**speaker amp. L-ch enable** **0: disable 1: enable**

0056 **SPK_CON2** **Speaker Control Register 2** **0004**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						**RG_SPK_OC_EN_L**	**RG_SPKAB_OC_EN_L**			**RG_SPKRCV_EN_L**			**RG_SPK_SLEW_L**			**RG_SPK_INTG_RST_L**
Type						RW	RW			RW			RW			RW
Reset						0	0			0			0	1		0

Bit(s)	Mnemonic	Name	Description
10	**RG_SPK_OC_EN_L**	RG_SPK_OC_EN_L	**claas D L-ch over-current protection enable** 0: disable 1: enable
9	**RG_SPKAB_OC_EN_L**	RG_SPKAB_OC_EN_L	**class AB mode L-ch Over-current protection enable** **0:disable 1:enable**
6	**RG_SPKRCV_EN_L**	RG_SPKRCV_EN_L	**speaker L-ch receiver mode voice bypass enable** 0: disable 1: enable
3:2	**RG_SPK_SLEW_L**	RG_SPK_SLEW_L	**Class D L-ch slew rate control** 00: 3/4 (default) 10.8n /8.3n (rise/fall) 01: 4/4 8.8n /6.3n 10: 1/4 16.4n /15n 11: 2/4 13.8n/12.6n
0	**RG_SPK_INTG_RST_L**	RG_SPK_INTG_RST_L	**speaker L-ch integrator reset control** 0: no reset 1: reset on

005E **SPK_CON6** **Speaker Control Register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPK_AB_OC_L_DEG**	**SPK_D_OC_L_DEG**			**SPK_OC_THD**		**SPK_OC_WND**									

005E **SPK_CON6** **Speaker Control Register 6** **0000**

Type	RO	RO			RW		RW									
Reset	0	0			0	0	0	0								

Bit(s)	Mnemonic	Name	Description
15	SPK_AB_OC_L_DEG	SPK_AB_OC_L_DEG	Class AB L-ch OC flag with deglitch 0: no OC for class AB mode 1: OC occurs for class AB mode
14	SPK_D_OC_L_DEG	SPK_D_OC_L_DEG	Class D L-ch OC flag with deglitch
11:10	SPK_OC_THD	SPK_OC_THD	Threshold setting in the decision window for SPK over current status 00: (4/8)*WND 01: (3/8)*WND 10: (2/8)*WND 11:(1/8)*WND
9:8	SPK_OC_WND	SPK_OC_WND	Decision window setting for SPK over current status 00: 16us 01: 32us 10: 64us 11:128us

0062 **SPK_CON8** **Speaker Control Register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_SPK_CCODE							
Type									RW							
Reset									0	0	0	0				

Bit(s)	Mnemonic	Name	Description
7:4	RG_SPK_CCODE	RG_SPK_CCODE	Class D modulation frequency control code (x000: 288k; x001:418.8k; x010:541k; x011:656k; x100:766k; x101:966k; x110:1.148M; x111:1.646M)

0064 **SPK_CON9** **Speaker Control Register 9** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_SPKPGA_GAIN											
Type					RW											
Reset					0	0	0	0								

Bit(s)	Mnemonic	Name	Description
11:8	RG_SPKPGA_GAIN	RG_SPKPGA_GAIN	speaker PGA gain control 0000:Mute 0001:0dB 0010:4dB 0011:5dB 0100:6dB 0101:7dB 0110:8dB 0111:9dB 1000:10dB 1001:11dB 1010:12dB 1011:13dB 1100:14dB 1101:15dB 1110:16dB 1111:17dB

006A **SPK_CON12** **Speaker Control Register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SPK_OUTSTG_EN_L_SW		SPK_EN_L_SW		SPK_DEPOP_EN_L_SW		SPKMODE_L_SW		SPK_RST_L_SW			
Type					RW		RW		RW		RW		RW			
Reset					0		0		0		0		0			

Bit(s)	Mnemonic	Name	Description
11	SPK_OUTSTG_EN_L_SW	SPK_OUTSTG_EN_L_SW	spekaer left channel output stage enable control 0: disable 1: enable
9	SPK_EN_L_SW	SPK_EN_L_SW	speaker amp. L-ch enable 0: disable 1: enable
7	SPK_DEPOP_EN_L_SW	SPK_DEPOP_EN_L_SW	class D L-ch mode depop enabled flag 0: depop disable 1: depop enable
5	SPKMODE_L_SW	SPKMODE_L_SW	speaker L-ch driver mode select 0: class D mode 1: class AB mode
3	SPK_RST_L_SW	SPK_RST_L_SW	Class D L-ch reset 0: not reset 1:reset

0070 **STRUP_CON13** **STRUP control register 13** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												STRUP_LONG_PRESS_EXT_EN	STRUP_LONG_PRESS_EXT_TD		STRUP_LONG_PRESS_EXT_SEL	
Type												RW	RW		RW	
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4	STRUP_LONG_PRESS_EXT_EN	STRUP_LONG_PRESS_EXT_EN	**Re-power on scenario function enable** 1'b0: disable long_press re-power on case 1'b1: enable long_press re-power on case
3:2	STRUP_LONG_PRESS_E	STRUP_LONG_PRESS_EXT_TD	**delay time selection** 2'b00: 0.5s 2'b01: 1s

Bit(s)	Mnemonic	Name	Description
	XT_TD		2'b10: 2s
1:0	STRUP_LONG_PRESS_EXT_SEL	STRUP_LONG_PRESS_EXT_SEL	**Re power-on scenario slection** 2'b00: debounce pwrkey 2'b01: after release pwrkey 2'b10: after release pwrkey and press pwrkey again

0078 **STRUP_CON17** **STRUP control register 17** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STRUP_PWROFF_STATUS_CLR
Type																W1C
Reset																0

Bit(s)	Mnemonic	Name	Description
0	STRUP_PWROFF_STATUS_CLR	STRUP_PWROFF_STATUS_CLR	**Clear power off status**

007A **STRUP_CON18** **STRUP control register 18** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RGS_VXO22_PG_PWROFF	RGS_VMCH_PG_PWROFF	RGS_VMC_PG_PWROFF	RGS_VUSB_PG_PWROFF	RGS_VM_PG_PWROFF	RGS_VM25_PG_PWROFF	RGS_VEMC33_PG_PWROFF	RGS_VGP2_PG_PWROFF	RGS_VIO28_PG_PWROFF	RGS_VIO18_PG_PWROFF	RGS_VSYS_PG_PWROFF	RGS_VPROC_PG_PWROFF	RGS_VCORE_PG_PWROFF	RGS_VADC18_PG_PWROFF
Type			RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
13	RGS_VXO22_PG	RGS_VXO22_PG_PWROFF	**power not good caused power-off**

Bit(s)	Mnemonic	Name	Description
	_PWROFF		
12	RGS_VMCH_PG_PWROFF	RGS_VMCH_PG_PWROFF	power not good caused power-off
11	RGS_VMC_PG_PWROFF	RGS_VMC_PG_PWROFF	power not good caused power-off
10	RGS_VUSB_PG_PWROFF	RGS_VUSB_PG_PWROFF	power not good caused power-off
9	RGS_VM_PG_PWROFF	RGS_VM_PG_PWROFF	power not good caused power-off
8	RGS_VM25_PG_PWROFF	RGS_VM25_PG_PWROFF	power not good caused power-off
7	RGS_VEMC33_PG_PWROFF	RGS_VEMC33_PG_PWROFF	power not good caused power-off
6	RGS_VGP2_PG_PWROFF	RGS_VGP2_PG_PWROFF	power not good caused power-off
5	RGS_VIO28_PG_PWROFF	RGS_VIO28_PG_PWROFF	power not good caused power-off
4	RGS_VIO18_PG_PWROFF	RGS_VIO18_PG_PWROFF	power not good caused power-off
3	RGS_VSYS_PG_PWROFF	RGS_VSYS_PG_PWROFF	power not good caused power-off
2	RGS_VPROC_PG_PWROFF	RGS_VPROC_PG_PWROFF	power not good caused power-off
1	RGS_VCORE_PG_PWROFF	RGS_VCORE_PG_PWROFF	power not good caused power-off
0	RGS_VADC18_PG_PWROFF	RGS_VADC18_PG_PWROFF	power not good caused power-off

007C **STRUP_CON19** **STRUP control register 19** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STRU						RGS_	RGS_	RGS_	RGS_	RGS_	RGS_	RGS_	RGS_	RGS_	RGS_

007C	STRUP_CON19	STRUP control register 19	0000

	P_PWROFF_HW_CLR_ENB						DDLO_PWROFF	DDLO_PWROFF	RTC_PWRBB_PWROFF	WDTRST_PWROFF	LONG_PRESS_PWROFF	THR_PWROFF	UVLO_PWROFF	VSYS_OC_PWROFF	VPROC_OC_PWROFF	VCORE_OC_PWROFF
Type	RW						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0						0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**STRUP_PWROFF_HW_CLR_ENB**	STRUP_PWROFF_HW_CLR_ENB	**HW auto clear last record power-off status when encounter new power-off** 0 : enable 1 : disable
9	**RGS_DDLO_PWROFF**	RGS_PWRCOND_PWROFF	
8	**RGS_DDLO_PWROFF**	RGS_DDLO_PWROFF	**DDLO low to high record**
7	**RGS_RTC_PWRBB_PWROFF**	RGS_RTC_PWRBB_PWROFF	**pwrbb caused power-off**
6	**RGS_WDTRST_PWROFF**	RGS_WDTRST_PWROFF	**watch-dog reset caused power-off**
5	**RGS_LONG_PRESS_PWROFF**	RGS_LONG_PRESS_PWROFF	**Long pressed reset caused power-off**
4	**RGS_THR_PWROFF**	RGS_THR_PWROFF	**thermal shutdown caused power-off**
3	**RGS_UVLO_PWROFF**	RGS_UVLO_PWROFF	**UVLO caused power-off**
2	**RGS_VSYS_OC_PWROFF**	RGS_VSYS_OC_PWROFF	**OC shutdown caused power-off**
1	**RGS_VPROC_OC_PWROFF**	RGS_VPROC_OC_PWROFF	**OC shutdown caused power-off**
0	**RGS_VCORE_OC_PWROFF**	RGS_VCORE_OC_PWROFF	**OC shutdown caused power-off**

011A **TOP_RST_MISC** **reset control misc** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RG_PWRKEY_RST_TD		RG_PWRRST_TMR_DIS	RG_PWRKEY_RST_EN	RG_HOMEKEY_RST_EN			RG_STRUP_MAN_RST_EN	RG_SYSRSTB_EN	
Type							RW		RW	RW	RW			RW	RW	
Reset							0	0	0	1	0			0	0	

Bit(s)	Name	Description
9:8	RG_PWRKEY_RST_TD	**PWRKEY long pressed time to issue reset**
7	RG_PWRRST_TMR_DIS	**PWRKEY long pressed timer dsiable and enable**
6	RG_PWRKEY_RST_EN	**PWRKEY long pressed reset enable**
5	RG_HOMEKEY_RST_EN	**RSTKEY long pressed reset enable**
2	RG_STRUP_MAN_RST_EN	**wdtrst STRUP circuit manual reset enable 1'b0: to wdtrst state 2 1'b1: to wdtrst state 1**
1	RG_SYSRSTB_EN	**wdtrst SYSRSTB(External Watchdog) reset from AP 1'b0: disable reset from AP 1'b1: enable wdtrst from AP**

0142 **CHRSTATUS** **CHR Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RO_BATON_UNDET	PCHR_CHRDET	VBAT_OV	FCHRKEY_DEB	PWRKEY_DEB	
Type											RO	RO	RO	RO	RO	
Reset											0	0	0	0	0	

Bit(s)	Name	Description
5	RO_BATON_UNDET	
4	PCHR_CHRDET	
3	VBAT_OV	
2	FCHRKEY_DEB	
1	PWRKEY_DEB	

0144 TDSEL_CON TDSEL_CON 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_PMU_TDSEL	RG_SPI_TDSEL		
Type													RW	RW		
Reset													0	0		

Bit(s)	Name	Description
3	RG_PMU_TDSEL	TDSEL
2	RG_SPI_TDSEL	RDSEL

0146 RDSEL_CON RDSEL_CON 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_PMU_RDSEL	RG_SPI_RDSEL		
Type													RW	RW		
Reset													0	0		

Bit(s)	Name	Description
3	RG_PMU_RDSEL	RDSEL
2	RG_SPI_RDSEL	SMT

0148 SMT_CON0 SMT_CON0 0004

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_SMT_RTC_32K1V8	RG_SMT_SRCLKEN	RG_SMT_INT	RG_SMT_SYSRSTB
Type													RW	RW	RW	RW
Reset													0	1	0	0

Bit(s)	Name	Description
3	RG_SMT_RTC_32K1V8	SMT
2	RG_SMT_SRCLKEN	SMT
1	RG_SMT_INT	SMT
0	RG_SMT_SYSRSTB	SMT

014A **SMT_CON1** **SMT_CON1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_SMT_SPI_MISO	RG_SMT_SPI_MOSI	RG_SMT_SPI_CSN	RG_SMT_SPI_CLK
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
3	RG_SMT_SPI_MISO	**SMT**
2	RG_SMT_SPI_MOSI	**SMT**
1	RG_SMT_SPI_CSN	**SMT**
0	RG_SMT_SPI_CLK	**SMT**

0152 **DRV_CON0** **DRV_CON0** **0CCC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_OCTL_RTC_32K1V8				RG_OCTL_SRCLKEN				RG_OCTL_INT			
Type					RW				RW				RW			
Reset					1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
11:8	RG_OCTL_RTC_32K1V8	**OC CTL, [11]:SR; [10]:E4; [9]:E2; [8]:null**
7:4	RG_OCTL_SRCLKEN	**OC CTL, [7]:SR; [6]:E4; [5]:E2; [4]:null**
3:0	RG_OCTL_INT	**OC CTL, [3]:SR; [2]:E4; [1]:E2; [0]:null**

0154 **DRV_CON1** **DRV_CON1** **CCCC**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_OCTL_SPI_MISO				RG_OCTL_SPI_MOSI				RG_OCTL_SPI_CSN				RG_OCTL_SPI_CLK			
Type	RW				RW				RW				RW			
Reset	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0

Bit(s)	Name	Description
15:12	RG_OCTL_SPI_MISO	**OC CTL, [15]:SR; [14]:E4; [13]:E2; [12]:null**
11:8	RG_OCTL_SPI_MOSI	**OC CTL, [11]:SR; [10]:E4; [9]:E2; [8]:null**
7:4	RG_OCTL_SPI_CSN	**OC CTL, [7]:SR; [6]:E4; [5]:E2; [4]:null**

Bit(s)	Name	Description
3:0	RG_OCTL_SPI_CLK	**OC CTL, [3]:SR; [2]:E4; [1]:E2; [0]:null**

0182 **FQMTR_CON0** **Frequency meter control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQMTR_EN												FQMTR_BUSY	FQMTR_TCKSEL		
Type	RW												RO	RW		
Reset	0												0	0	0	0

Bit(s)	Mnemonic	Name	Description
15	**FQMTR_EN**	FQMTR_EN	**Enables frequency meter**
3	**FQMTR_BUSY**	FQMTR_BUSY	**Frequency meter busy status**
2:0	**FQMTR_TCKSEL**	FQMTR_TCKSEL	**Frequency meter target (measured) clock selection**

0184 **FQMTR_CON1** **Frequency meter control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQMTR_WINSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**FQMTR_WINSET**	FQMTR_WINSET	**Frequency meter window setting (= numbers of FIXED clock cycles)**

0186 **FQMTR_CON2** **Frequency meter control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FQMTR_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
15:0	FQMTR_DATA	FQMTR_DATA	Frequency meter data to be read out

0210 **VPROC_CON2** **VPROC control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_VPROC_MODESET								
Type								RW								
Reset								0								

Bit(s)	Name	Description
8	RG_VPROC_MODESET	1: force PWM mode 0: auto mode

0212 **VPROC_CON3** **VPROC control register 3** **0020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											QI_VPROC_VSLEEP					
Type											RW					
Reset											1	0				

Bit(s)	Name	Description
5:4	QI_VPROC_VSLEEP	**Sleep mode voltage selection** 00: 0.7V 01: 0.75V 10: 0.85V 11: 0.9V

021A **VPROC_CON7** **VPROC control register 7** **2001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			QI_VPROC_EN													VPROC_EN
Type			RO													RW
Reset			1													1

Bit(s)	Name	Description
13	QI_VPROC_EN	**Enable signal** 0: Disable 1: Enable
0	VPROC_EN	**Enable** 0: Disable 1: Enable

021E **VPROC_CON9** **VPROC control register 9** **0048**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VPROC_VOSEL						
Type										RW						
Reset										1	0	0	1	0	0	0

Bit(s)	Name	Description
6:0	VPROC_VOSEL	**VOUT selection in register mode** 0000000: 0.70000V 0000001: 0.70625V 0000010: 0.71250V 0000011: 0.71875V 0000100: 0.72500V 0000101: 0.73125V 0000110: 0.73750V 0000111: 0.74375V 0001000: 0.75000V 0001001: 0.75625V 0001010: 0.76250V 0001011: 0.76875V 0001100: 0.77500V 0001101: 0.78125V 0001110: 0.78750V 0001111: 0.79375V 0010000: 0.80000V 0010001: 0.80625V 0010010: 0.81250V 0010011: 0.81875V 0010100: 0.82500V 0010101: 0.83125V 0010110: 0.83750V 0010111: 0.84375V 0011000: 0.85000V 0011001: 0.85625V 0011010: 0.86250V 0011011: 0.86875V 0011100: 0.87500V 0011101: 0.88125V 0011110: 0.88750V 0011111: 0.89375V 0100000: 0.90000V 0100001: 0.90625V 0100010: 0.91250V 0100011: 0.91875V 0100100: 0.92500V

Bit(s)	Name	Description
		0100101: 0.93125V 0100110: 0.93750V 0100111: 0.94375V 0101000: 0.95000V 0101001: 0.95625V 0101010: 0.96250V 0101011: 0.96875V 0101100: 0.97500V 0101101: 0.98125V 0101110: 0.98750V 0101111: 0.99375V 0110000: 1.00000V 0110001: 1.00625V 0110010: 1.01250V 0110011: 1.01875V 0110100: 1.02500V 0110101: 1.03125V 0110110: 1.03750V 0110111: 1.04375V 0111000: 1.05000V 0111001: 1.05625V 0111010: 1.06250V 0111011: 1.06875V 0111100: 1.07500V 0111101: 1.08125V 0111110: 1.08750V 0111111: 1.09375V 1000000: 1.10000V 1000001: 1.10625V 1000010: 1.11250V 1000011: 1.11875V 1000100: 1.12500V 1000101: 1.13125V 1000110: 1.13750V 1000111: 1.14375V 1001000: 1.15000V 1001001: 1.15625V 1001010: 1.16250V 1001011: 1.16875V 1001100: 1.17500V 1001101: 1.18125V 1001110: 1.18750V 1001111: 1.19375V 1010000: 1.20000V 1010001: 1.20625V 1010010: 1.21250V 1010011: 1.21875V 1010100: 1.22500V 1010101: 1.23125V 1010110: 1.23750V 1010111: 1.24375V 1011000: 1.25000V 1011001: 1.25625V 1011010: 1.26250V 1011011: 1.26875V 1011100: 1.27500V 1011101: 1.28125V 1011110: 1.28750V 1011111: 1.29375V 1100000: 1.30000V 1100001: 1.30625V 1100010: 1.31250V

Bit(s)	Name	Description
		1100011: 1.31875V 1100100: 1.32500V 1100101: 1.33125V 1100110: 1.33750V 1100111: 1.34375V 1101000: 1.35000V 1101001: 1.35625V 1101010: 1.36250V 1101011: 1.36875V 1101100: 1.37500V 1101101: 1.38125V 1101110: 1.38750V 1101111: 1.39375V 1110000: 1.40000V 1110001: 1.40625V 1110010: 1.41250V 1110011: 1.41875V 1110100: 1.42500V 1110101: 1.43125V 1110110: 1.43750V 1110111: 1.44375V 1111000: 1.45000V 1111001: 1.45625V 1111010: 1.46250V 1111011: 1.46875V 1111100: 1.47500V 1111101: 1.48125V 1111110: 1.48750V 1111111: 1.49375V

0220 **VPROC_CON10** **VPROC control register 10** **0048**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VPROC_VOSEL_ON						
Type										RW						
Reset										1	0	0	1	0	0	0

Bit(s)	Name	Description
		VOUT selection in normal mode
6:0	VPROC_VOSEL_ON	0000000: 0.70000V 0000001: 0.70625V 0000010: 0.71250V 0000011: 0.71875V 0000100: 0.72500V 0000101: 0.73125V 0000110: 0.73750V 0000111: 0.74375V 0001000: 0.75000V 0001001: 0.75625V 0001010: 0.76250V 0001011: 0.76875V 0001100: 0.77500V 0001101: 0.78125V 0001110: 0.78750V 0001111: 0.79375V 0010000: 0.80000V

Bit(s)	Name	Description
		0010001: 0.80625V 0010010: 0.81250V 0010011: 0.81875V 0010100: 0.82500V 0010101: 0.83125V 0010110: 0.83750V 0010111: 0.84375V 0011000: 0.85000V 0011001: 0.85625V 0011010: 0.86250V 0011011: 0.86875V 0011100: 0.87500V 0011101: 0.88125V 0011110: 0.88750V 0011111: 0.89375V 0100000: 0.90000V 0100001: 0.90625V 0100010: 0.91250V 0100011: 0.91875V 0100100: 0.92500V 0100101: 0.93125V 0100110: 0.93750V 0100111: 0.94375V 0101000: 0.95000V 0101001: 0.95625V 0101010: 0.96250V 0101011: 0.96875V 0101100: 0.97500V 0101101: 0.98125V 0101110: 0.98750V 0101111: 0.99375V 0110000: 1.00000V 0110001: 1.00625V 0110010: 1.01250V 0110011: 1.01875V 0110100: 1.02500V 0110101: 1.03125V 0110110: 1.03750V 0110111: 1.04375V 0111000: 1.05000V 0111001: 1.05625V 0111010: 1.06250V 0111011: 1.06875V 0111100: 1.07500V 0111101: 1.08125V 0111110: 1.08750V 0111111: 1.09375V 1000000: 1.10000V 1000001: 1.10625V 1000010: 1.11250V 1000011: 1.11875V 1000100: 1.12500V 1000101: 1.13125V 1000110: 1.13750V 1000111: 1.14375V 1001000: 1.15000V 1001001: 1.15625V 1001010: 1.16250V 1001011: 1.16875V 1001100: 1.17500V 1001101: 1.18125V 1001110: 1.18750V

Bit(s)	Name	Description
		1001111: 1.19375V 1010000: 1.20000V 1010001: 1.20625V 1010010: 1.21250V 1010011: 1.21875V 1010100: 1.22500V 1010101: 1.23125V 1010110: 1.23750V 1010111: 1.24375V 1011000: 1.25000V 1011001: 1.25625V 1011010: 1.26250V 1011011: 1.26875V 1011100: 1.27500V 1011101: 1.28125V 1011110: 1.28750V 1011111: 1.29375V 1100000: 1.30000V 1100001: 1.30625V 1100010: 1.31250V 1100011: 1.31875V 1100100: 1.32500V 1100101: 1.33125V 1100110: 1.33750V 1100111: 1.34375V 1101000: 1.35000V 1101001: 1.35625V 1101010: 1.36250V 1101011: 1.36875V 1101100: 1.37500V 1101101: 1.38125V 1101110: 1.38750V 1101111: 1.39375V 1110000: 1.40000V 1110001: 1.40625V 1110010: 1.41250V 1110011: 1.41875V 1110100: 1.42500V 1110101: 1.43125V 1110110: 1.43750V 1110111: 1.44375V 1111000: 1.45000V 1111001: 1.45625V 1111010: 1.46250V 1111011: 1.46875V 1111100: 1.47500V 1111101: 1.48125V 1111110: 1.48750V 1111111: 1.49375V

0222 **VPROC_CON11** **VPROC control register 11** **0048**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VPROC_VOSEL_SLEEP						
Type										RW						
Reset										1	0	0	1	0	0	0

Bit(s)	Name	Description
6:0	VPROC_VOSEL_SLEEP	**VOUT selection in sleep mode** 0000000: 0.70000V 0000001: 0.70625V 0000010: 0.71250V 0000011: 0.71875V 0000100: 0.72500V 0000101: 0.73125V 0000110: 0.73750V 0000111: 0.74375V 0001000: 0.75000V 0001001: 0.75625V 0001010: 0.76250V 0001011: 0.76875V 0001100: 0.77500V 0001101: 0.78125V 0001110: 0.78750V 0001111: 0.79375V 0010000: 0.80000V 0010001: 0.80625V 0010010: 0.81250V 0010011: 0.81875V 0010100: 0.82500V 0010101: 0.83125V 0010110: 0.83750V 0010111: 0.84375V 0011000: 0.85000V 0011001: 0.85625V 0011010: 0.86250V 0011011: 0.86875V 0011100: 0.87500V 0011101: 0.88125V 0011110: 0.88750V 0011111: 0.89375V 0100000: 0.90000V 0100001: 0.90625V 0100010: 0.91250V 0100011: 0.91875V 0100100: 0.92500V 0100101: 0.93125V 0100110: 0.93750V 0100111: 0.94375V 0101000: 0.95000V 0101001: 0.95625V 0101010: 0.96250V 0101011: 0.96875V 0101100: 0.97500V 0101101: 0.98125V 0101110: 0.98750V 0101111: 0.99375V 0110000: 1.00000V 0110001: 1.00625V 0110010: 1.01250V 0110011: 1.01875V 0110100: 1.02500V 0110101: 1.03125V 0110110: 1.03750V 0110111: 1.04375V 0111000: 1.05000V 0111001: 1.05625V 0111010: 1.06250V 0111011: 1.06875V

Bit(s)	Name	Description
		0111100: 1.07500V 0111101: 1.08125V 0111110: 1.08750V 0111111: 1.09375V 1000000: 1.10000V 1000001: 1.10625V 1000010: 1.11250V 1000011: 1.11875V 1000100: 1.12500V 1000101: 1.13125V 1000110: 1.13750V 1000111: 1.14375V 1001000: 1.15000V 1001001: 1.15625V 1001010: 1.16250V 1001011: 1.16875V 1001100: 1.17500V 1001101: 1.18125V 1001110: 1.18750V 1001111: 1.19375V 1010000: 1.20000V 1010001: 1.20625V 1010010: 1.21250V 1010011: 1.21875V 1010100: 1.22500V 1010101: 1.23125V 1010110: 1.23750V 1010111: 1.24375V 1011000: 1.25000V 1011001: 1.25625V 1011010: 1.26250V 1011011: 1.26875V 1011100: 1.27500V 1011101: 1.28125V 1011110: 1.28750V 1011111: 1.29375V 1100000: 1.30000V 1100001: 1.30625V 1100010: 1.31250V 1100011: 1.31875V 1100100: 1.32500V 1100101: 1.33125V 1100110: 1.33750V 1100111: 1.34375V 1101000: 1.35000V 1101001: 1.35625V 1101010: 1.36250V 1101011: 1.36875V 1101100: 1.37500V 1101101: 1.38125V 1101110: 1.38750V 1101111: 1.39375V 1110000: 1.40000V 1110001: 1.40625V 1110010: 1.41250V 1110011: 1.41875V 1110100: 1.42500V 1110101: 1.43125V 1110110: 1.43750V 1110111: 1.44375V 1111000: 1.45000V 1111001: 1.45625V

Bit(s)	Name	Description
		1111010: 1.46250V 1111011: 1.46875V 1111100: 1.47500V 1111101: 1.48125V 1111110: 1.48750V 1111111: 1.49375V

0224 **VPROC_CON12** **VPROC control register 12** **0048**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										NI_VPROC_VOSEL						
Type										RO						
Reset										1	0	0	1	0	0	0

Bit(s)	Name	Description
		VOUT selection
6:0	NI_VPROC_VOSEL	0000000: 0.70000V 0000001: 0.70625V 0000010: 0.71250V 0000011: 0.71875V 0000100: 0.72500V 0000101: 0.73125V 0000110: 0.73750V 0000111: 0.74375V 0001000: 0.75000V 0001001: 0.75625V 0001010: 0.76250V 0001011: 0.76875V 0001100: 0.77500V 0001101: 0.78125V 0001110: 0.78750V 0001111: 0.79375V 0010000: 0.80000V 0010001: 0.80625V 0010010: 0.81250V 0010011: 0.81875V 0010100: 0.82500V 0010101: 0.83125V 0010110: 0.83750V 0010111: 0.84375V 0011000: 0.85000V 0011001: 0.85625V 0011010: 0.86250V 0011011: 0.86875V 0011100: 0.87500V 0011101: 0.88125V 0011110: 0.88750V 0011111: 0.89375V 0100000: 0.90000V 0100001: 0.90625V 0100010: 0.91250V 0100011: 0.91875V 0100100: 0.92500V 0100101: 0.93125V 0100110: 0.93750V 0100111: 0.94375V

Bit(s)	Name	Description
		0101000: 0.95000V 0101001: 0.95625V 0101010: 0.96250V 0101011: 0.96875V 0101100: 0.97500V 0101101: 0.98125V 0101110: 0.98750V 0101111: 0.99375V 0110000: 1.00000V 0110001: 1.00625V 0110010: 1.01250V 0110011: 1.01875V 0110100: 1.02500V 0110101: 1.03125V 0110110: 1.03750V 0110111: 1.04375V 0111000: 1.05000V 0111001: 1.05625V 0111010: 1.06250V 0111011: 1.06875V 0111100: 1.07500V 0111101: 1.08125V 0111110: 1.08750V 0111111: 1.09375V 1000000: 1.10000V 1000001: 1.10625V 1000010: 1.11250V 1000011: 1.11875V 1000100: 1.12500V 1000101: 1.13125V 1000110: 1.13750V 1000111: 1.14375V 1001000: 1.15000V 1001001: 1.15625V 1001010: 1.16250V 1001011: 1.16875V 1001100: 1.17500V 1001101: 1.18125V 1001110: 1.18750V 1001111: 1.19375V 1010000: 1.20000V 1010001: 1.20625V 1010010: 1.21250V 1010011: 1.21875V 1010100: 1.22500V 1010101: 1.23125V 1010110: 1.23750V 1010111: 1.24375V 1011000: 1.25000V 1011001: 1.25625V 1011010: 1.26250V 1011011: 1.26875V 1011100: 1.27500V 1011101: 1.28125V 1011110: 1.28750V 1011111: 1.29375V 1100000: 1.30000V 1100001: 1.30625V 1100010: 1.31250V 1100011: 1.31875V 1100100: 1.32500V 1100101: 1.33125V

Bit(s)	Name	Description
		1100110: 1.33750V 1100111: 1.34375V 1101000: 1.35000V 1101001: 1.35625V 1101010: 1.36250V 1101011: 1.36875V 1101100: 1.37500V 1101101: 1.38125V 1101110: 1.38750V 1101111: 1.39375V 1110000: 1.40000V 1110001: 1.40625V 1110010: 1.41250V 1110011: 1.41875V 1110100: 1.42500V 1110101: 1.43125V 1110110: 1.43750V 1110111: 1.44375V 1111000: 1.45000V 1111001: 1.45625V 1111010: 1.46250V 1111011: 1.46875V 1111100: 1.47500V 1111101: 1.48125V 1111110: 1.48750V 1111111: 1.49375V

0236 VSYS_CON2 VSYS control register 2 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RG_VSYS_MODESET								
Type								RW								
Reset								0								

Bit(s)	Name	Description
8	RG_VSYS_MODESET	1: force PWM mode 0: auto mode

0240 VSYS_CON7 VSYS control register 7 2001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			QI_VSYS_EN													VSYS_EN
Type			RO													RW
Reset			1													1

Bit(s)	Name	Description
13	QI_VSYS_EN	**Enable signal**
0	VSYS_EN	**Enable**

0244 VSYS_CON9 VSYS control register 9 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VSYS_VOSEL						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	VSYS_VOSEL	**VOUT selection in register mode** 0000000: 1.40000V 0000001: 1.41250V 0000010: 1.42500V 0000011: 1.43750V 0000100: 1.45000V 0000101: 1.46250V 0000110: 1.47500V 0000111: 1.48750V 0001000: 1.50000V 0001001: 1.51250V 0001010: 1.52500V 0001011: 1.53750V 0001100: 1.55000V 0001101: 1.56250V 0001110: 1.57500V 0001111: 1.58750V 0010000: 1.60000V 0010001: 1.61250V 0010010: 1.62500V 0010011: 1.63750V 0010100: 1.65000V 0010101: 1.66250V 0010110: 1.67500V 0010111: 1.68750V 0011000: 1.70000V 0011001: 1.71250V 0011010: 1.72500V 0011011: 1.73750V 0011100: 1.75000V 0011101: 1.76250V 0011110: 1.77500V 0011111: 1.78750V 0100000: 1.80000V 0100001: 1.81250V 0100010: 1.82500V 0100011: 1.83750V 0100100: 1.85000V 0100101: 1.86250V 0100110: 1.87500V 0100111: 1.88750V 0101000: 1.90000V 0101001: 1.91250V 0101010: 1.92500V 0101011: 1.93750V

Bit(s)	Name	Description
		0101100: 1.95000V 0101101: 1.96250V 0101110: 1.97500V 0101111: 1.98750V 0110000: 2.00000V 0110001: 2.01250V 0110010: 2.02500V 0110011: 2.03750V 0110100: 2.05000V 0110101: 2.06250V 0110110: 2.07500V 0110111: 2.08750V 0111000: 2.10000V 0111001: 2.11250V 0111010: 2.12500V 0111011: 2.13750V 0111100: 2.15000V 0111101: 2.16250V 0111110: 2.17500V 0111111: 2.18750V 1000000: 2.20000V 1000001: 2.21250V 1000010: 2.22500V 1000011: 2.23750V 1000100: 2.25000V 1000101: 2.26250V 1000110: 2.27500V 1000111: 2.28750V 1001000: 2.30000V 1001001: 2.31250V 1001010: 2.32500V 1001011: 2.33750V 1001100: 2.35000V 1001101: 2.36250V 1001110: 2.37500V 1001111: 2.38750V 1010000: 2.40000V 1010001: 2.41250V 1010010: 2.42500V 1010011: 2.43750V 1010100: 2.45000V 1010101: 2.46250V 1010110: 2.47500V 1010111: 2.48750V 1011000: 2.50000V 1011001: 2.51250V 1011010: 2.52500V 1011011: 2.53750V 1011100: 2.55000V 1011101: 2.56250V 1011110: 2.57500V 1011111: 2.58750V 1100000: 2.60000V 1100001: 2.61250V 1100010: 2.62500V 1100011: 2.63750V 1100100: 2.65000V 1100101: 2.66250V 1100110: 2.67500V 1100111: 2.68750V 1101000: 2.70000V 1101001: 2.71250V

Bit(s)	Name	Description
		1101010: 2.72500V 1101011: 2.73750V 1101100: 2.75000V 1101101: 2.76250V 1101110: 2.77500V 1101111: 2.78750V 1110000: 2.80000V 1110001: 2.81250V 1110010: 2.82500V 1110011: 2.83750V 1110100: 2.85000V 1110101: 2.86250V 1110110: 2.87500V 1110111: 2.88750V 1111000: 2.90000V 1111001: 2.91250V 1111010: 2.92500V 1111011: 2.93750V 1111100: 2.95000V 1111101: 2.96250V 1111110: 2.97500V 1111111: 2.98750V

0246 **VSYS_CON10** **VSYS control register 10** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VSYS_VOSEL_ON						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	VSYS_VOSEL_ON	**VOUT selection in normal mode** 0000000: 1.40000V 0000001: 1.41250V 0000010: 1.42500V 0000011: 1.43750V 0000100: 1.45000V 0000101: 1.46250V 0000110: 1.47500V 0000111: 1.48750V 0001000: 1.50000V 0001001: 1.51250V 0001010: 1.52500V 0001011: 1.53750V 0001100: 1.55000V 0001101: 1.56250V 0001110: 1.57500V 0001111: 1.58750V 0010000: 1.60000V 0010001: 1.61250V 0010010: 1.62500V 0010011: 1.63750V 0010100: 1.65000V 0010101: 1.66250V 0010110: 1.67500V 0010111: 1.68750V

Bit(s)	Name	Description
		0011000: 1.70000V 0011001: 1.71250V 0011010: 1.72500V 0011011: 1.73750V 0011100: 1.75000V 0011101: 1.76250V 0011110: 1.77500V 0011111: 1.78750V 0100000: 1.80000V 0100001: 1.81250V 0100010: 1.82500V 0100011: 1.83750V 0100100: 1.85000V 0100101: 1.86250V 0100110: 1.87500V 0100111: 1.88750V 0101000: 1.90000V 0101001: 1.91250V 0101010: 1.92500V 0101011: 1.93750V 0101100: 1.95000V 0101101: 1.96250V 0101110: 1.97500V 0101111: 1.98750V 0110000: 2.00000V 0110001: 2.01250V 0110010: 2.02500V 0110011: 2.03750V 0110100: 2.05000V 0110101: 2.06250V 0110110: 2.07500V 0110111: 2.08750V 0111000: 2.10000V 0111001: 2.11250V 0111010: 2.12500V 0111011: 2.13750V 0111100: 2.15000V 0111101: 2.16250V 0111110: 2.17500V 0111111: 2.18750V 1000000: 2.20000V 1000001: 2.21250V 1000010: 2.22500V 1000011: 2.23750V 1000100: 2.25000V 1000101: 2.26250V 1000110: 2.27500V 1000111: 2.28750V 1001000: 2.30000V 1001001: 2.31250V 1001010: 2.32500V 1001011: 2.33750V 1001100: 2.35000V 1001101: 2.36250V 1001110: 2.37500V 1001111: 2.38750V 1010000: 2.40000V 1010001: 2.41250V 1010010: 2.42500V 1010011: 2.43750V 1010100: 2.45000V 1010101: 2.46250V

Bit(s)	Name	Description
		1010110: 2.47500V 1010111: 2.48750V 1011000: 2.50000V 1011001: 2.51250V 1011010: 2.52500V 1011011: 2.53750V 1011100: 2.55000V 1011101: 2.56250V 1011110: 2.57500V 1011111: 2.58750V 1100000: 2.60000V 1100001: 2.61250V 1100010: 2.62500V 1100011: 2.63750V 1100100: 2.65000V 1100101: 2.66250V 1100110: 2.67500V 1100111: 2.68750V 1101000: 2.70000V 1101001: 2.71250V 1101010: 2.72500V 1101011: 2.73750V 1101100: 2.75000V 1101101: 2.76250V 1101110: 2.77500V 1101111: 2.78750V 1110000: 2.80000V 1110001: 2.81250V 1110010: 2.82500V 1110011: 2.83750V 1110100: 2.85000V 1110101: 2.86250V 1110110: 2.87500V 1110111: 2.88750V 1111000: 2.90000V 1111001: 2.91250V 1111010: 2.92500V 1111011: 2.93750V 1111100: 2.95000V 1111101: 2.96250V 1111110: 2.97500V 1111111: 2.98750V

0248 VSYS_CON11 VSYS control register 11 0040

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VSYS_VOSEL_SLEEP						
Type										RW						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
		VOUT selection in sleep mode
6:0	VSYS_VOSEL_SLEEP	0000000: 1.40000V 0000001: 1.41250V 0000010: 1.42500V 0000011: 1.43750V 0000100: 1.45000V

Bit(s)	Name	Description
		0000101: 1.46250V 0000110: 1.47500V 0000111: 1.48750V 0001000: 1.50000V 0001001: 1.51250V 0001010: 1.52500V 0001011: 1.53750V 0001100: 1.55000V 0001101: 1.56250V 0001110: 1.57500V 0001111: 1.58750V 0010000: 1.60000V 0010001: 1.61250V 0010010: 1.62500V 0010011: 1.63750V 0010100: 1.65000V 0010101: 1.66250V 0010110: 1.67500V 0010111: 1.68750V 0011000: 1.70000V 0011001: 1.71250V 0011010: 1.72500V 0011011: 1.73750V 0011100: 1.75000V 0011101: 1.76250V 0011110: 1.77500V 0011111: 1.78750V 0100000: 1.80000V 0100001: 1.81250V 0100010: 1.82500V 0100011: 1.83750V 0100100: 1.85000V 0100101: 1.86250V 0100110: 1.87500V 0100111: 1.88750V 0101000: 1.90000V 0101001: 1.91250V 0101010: 1.92500V 0101011: 1.93750V 0101100: 1.95000V 0101101: 1.96250V 0101110: 1.97500V 0101111: 1.98750V 0110000: 2.00000V 0110001: 2.01250V 0110010: 2.02500V 0110011: 2.03750V 0110100: 2.05000V 0110101: 2.06250V 0110110: 2.07500V 0110111: 2.08750V 0111000: 2.10000V 0111001: 2.11250V 0111010: 2.12500V 0111011: 2.13750V 0111100: 2.15000V 0111101: 2.16250V 0111110: 2.17500V 0111111: 2.18750V 1000000: 2.20000V 1000001: 2.21250V 1000010: 2.22500V

Bit(s)	Name	Description
		1000011: 2.23750V 1000100: 2.25000V 1000101: 2.26250V 1000110: 2.27500V 1000111: 2.28750V 1001000: 2.30000V 1001001: 2.31250V 1001010: 2.32500V 1001011: 2.33750V 1001100: 2.35000V 1001101: 2.36250V 1001110: 2.37500V 1001111: 2.38750V 1010000: 2.40000V 1010001: 2.41250V 1010010: 2.42500V 1010011: 2.43750V 1010100: 2.45000V 1010101: 2.46250V 1010110: 2.47500V 1010111: 2.48750V 1011000: 2.50000V 1011001: 2.51250V 1011010: 2.52500V 1011011: 2.53750V 1011100: 2.55000V 1011101: 2.56250V 1011110: 2.57500V 1011111: 2.58750V 1100000: 2.60000V 1100001: 2.61250V 1100010: 2.62500V 1100011: 2.63750V 1100100: 2.65000V 1100101: 2.66250V 1100110: 2.67500V 1100111: 2.68750V 1101000: 2.70000V 1101001: 2.71250V 1101010: 2.72500V 1101011: 2.73750V 1101100: 2.75000V 1101101: 2.76250V 1101110: 2.77500V 1101111: 2.78750V 1110000: 2.80000V 1110001: 2.81250V 1110010: 2.82500V 1110011: 2.83750V 1110100: 2.85000V 1110101: 2.86250V 1110110: 2.87500V 1110111: 2.88750V 1111000: 2.90000V 1111001: 2.91250V 1111010: 2.92500V 1111011: 2.93750V 1111100: 2.95000V 1111101: 2.96250V 1111110: 2.97500V 1111111: 2.98750V

024A **VSYS_CON12** **VSYS control register 12** **0040**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										NI_VSYS_VOSEL						
Type										RO						
Reset										1	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	NI_VSYS_VOSEL	**VOUT selection** 0000000: 1.40000V 0000001: 1.41250V 0000010: 1.42500V 0000011: 1.43750V 0000100: 1.45000V 0000101: 1.46250V 0000110: 1.47500V 0000111: 1.48750V 0001000: 1.50000V 0001001: 1.51250V 0001010: 1.52500V 0001011: 1.53750V 0001100: 1.55000V 0001101: 1.56250V 0001110: 1.57500V 0001111: 1.58750V 0010000: 1.60000V 0010001: 1.61250V 0010010: 1.62500V 0010011: 1.63750V 0010100: 1.65000V 0010101: 1.66250V 0010110: 1.67500V 0010111: 1.68750V 0011000: 1.70000V 0011001: 1.71250V 0011010: 1.72500V 0011011: 1.73750V 0011100: 1.75000V 0011101: 1.76250V 0011110: 1.77500V 0011111: 1.78750V 0100000: 1.80000V 0100001: 1.81250V 0100010: 1.82500V 0100011: 1.83750V 0100100: 1.85000V 0100101: 1.86250V 0100110: 1.87500V 0100111: 1.88750V 0101000: 1.90000V 0101001: 1.91250V 0101010: 1.92500V 0101011: 1.93750V 0101100: 1.95000V 0101101: 1.96250V 0101110: 1.97500V 0101111: 1.98750V

Bit(s)	Name	Description
		0110000: 2.00000V 0110001: 2.01250V 0110010: 2.02500V 0110011: 2.03750V 0110100: 2.05000V 0110101: 2.06250V 0110110: 2.07500V 0110111: 2.08750V 0111000: 2.10000V 0111001: 2.11250V 0111010: 2.12500V 0111011: 2.13750V 0111100: 2.15000V 0111101: 2.16250V 0111110: 2.17500V 0111111: 2.18750V 1000000: 2.20000V 1000001: 2.21250V 1000010: 2.22500V 1000011: 2.23750V 1000100: 2.25000V 1000101: 2.26250V 1000110: 2.27500V 1000111: 2.28750V 1001000: 2.30000V 1001001: 2.31250V 1001010: 2.32500V 1001011: 2.33750V 1001100: 2.35000V 1001101: 2.36250V 1001110: 2.37500V 1001111: 2.38750V 1010000: 2.40000V 1010001: 2.41250V 1010010: 2.42500V 1010011: 2.43750V 1010100: 2.45000V 1010101: 2.46250V 1010110: 2.47500V 1010111: 2.48750V 1011000: 2.50000V 1011001: 2.51250V 1011010: 2.52500V 1011011: 2.53750V 1011100: 2.55000V 1011101: 2.56250V 1011110: 2.57500V 1011111: 2.58750V 1100000: 2.60000V 1100001: 2.61250V 1100010: 2.62500V 1100011: 2.63750V 1100100: 2.65000V 1100101: 2.66250V 1100110: 2.67500V 1100111: 2.68750V 1101000: 2.70000V 1101001: 2.71250V 1101010: 2.72500V 1101011: 2.73750V 1101100: 2.75000V 1101101: 2.76250V

Bit(s)	Name	Description
		1101110: 2.77500V 1101111: 2.78750V 1110000: 2.80000V 1110001: 2.81250V 1110010: 2.82500V 1110011: 2.83750V 1110100: 2.85000V 1110101: 2.86250V 1110110: 2.87500V 1110111: 2.88750V 1111000: 2.90000V 1111001: 2.91250V 1111010: 2.92500V 1111011: 2.93750V 1111100: 2.95000V 1111101: 2.96250V 1111110: 2.97500V 1111111: 2.98750V

0258 **BUCK_OC_CON0** **BUCK_OC control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														BUCK_VPROC_OC_STATUS	BUCK_VCORE_OC_STATUS	BUCK_VSYS_OC_STATUS
Type														RO	RO	RO
Reset														0	0	0

Bit(s)	Name	Description
2	BUCK_VPROC_OC_STATUS	**OC status condition** 0: No OC 1: OC occurs
1	BUCK_VCORE_OC_STATUS	**OC status condition** 0: No OC 1: OC occurs
0	BUCK_VSYS_OC_STATUS	**OC status condition** 0: No OC 1: OC occurs

025E **BUCK_OC_CON3** **BUCK_OC control register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														BUCK_VPROC	BUCK_VCORE	BUCK_VSYS

025E **BUCK_OC_CON3** **BUCK_OC control register 3** **0000**

														OC_OC_FLAG_CLR	RE_OC_FLAG_CLR	S_OC_FLAG_CLR
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	BUCK_VPROC_OC_FLAG_CLR	**1: clear OC status** 0: keep OC status
1	BUCK_VCORE_OC_FLAG_CLR	**1: clear OC status** 0: keep OC status
0	BUCK_VSYS_OC_FLAG_CLR	**1: clear OC status** 0: keep OC status

0260 **BUCK_OC_CON4** **BUCK_OC control register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														BUCK_VPROC_OC_FLAG_CLR_SEL	BUCK_VCORE_OC_FLAG_CLR_SEL	BUCK_VSYS_OC_FLAG_CLR_SEL
Type														RW	RW	RW
Reset														0	0	0

Bit(s)	Name	Description
2	BUCK_VPROC_OC_FLAG_CLR_SEL	**1: SW clear OC status** 0: HW clear OC status
1	BUCK_VCORE_OC_FLAG_CLR_SEL	**1: SW clear OC status** 0: HW clear OC status
0	BUCK_VSYS_OC_FLAG_CLR_SEL	**1: SW clear OC status** 0: HW clear OC status

0304 **VCORE_CON2** **VCORE control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Nam								RG								

0304 **VCORE_CON2** **VCORE control register 2** **0000**

Name								_VCORE_MODESET								
Type								RW								
Reset								0								

Bit(s)	Mnemonic	Name	Description
8	RG_VCORE_MODESET	RG_VCORE_MODESET	1: force PWM mode 0: auto mode

0306 **VCORE_CON3** **VCORE control register 3** **0020**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											RG_VCORE_VSLEEP					
Type											RW					
Reset											1	0				

Bit(s)	Mnemonic	Name	Description
5:4	RG_VCORE_VSLEEP	QI_VCORE_VSLEEP	**Sleep mode voltage selection** 00: 0.7V 01: 0.75V 10: 0.85V 11: 0.9V

030E **VCORE_CON7** **VCORE control register 7** **2001**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			QI_VCORE_EN													VCORE_EN
Type			RO													RW
Reset			1													1

Bit(s)	Mnemonic	Name	Description
13	QI_VCORE_EN	QI_VCORE_EN	**Enable signal** 0: Disable

Bit(s)	Mnemonic	Name	Description
0	**VCORE_EN**	VCORE_EN	1: Enable **Enable** 0: Disable 1: Enable

0312 **VCORE_CON9** **VCORE control register 9** **0048**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VCORE_VOSEL						
Type										RW						
Reset										1	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0	**VCORE_VOSEL**	VCORE_VOSEL	**VOUT selection in register mode** 0000000: 0.70000V 0000001: 0.70625V 0000010: 0.71250V 0000011: 0.71875V 0000100: 0.72500V 0000101: 0.73125V 0000110: 0.73750V 0000111: 0.74375V 0001000: 0.75000V 0001001: 0.75625V 0001010: 0.76250V 0001011: 0.76875V 0001100: 0.77500V 0001101: 0.78125V 0001110: 0.78750V 0001111: 0.79375V 0010000: 0.80000V 0010001: 0.80625V 0010010: 0.81250V 0010011: 0.81875V 0010100: 0.82500V 0010101: 0.83125V 0010110: 0.83750V 0010111: 0.84375V 0011000: 0.85000V 0011001: 0.85625V 0011010: 0.86250V 0011011: 0.86875V 0011100: 0.87500V 0011101: 0.88125V 0011110: 0.88750V 0011111: 0.89375V 0100000: 0.90000V 0100001: 0.90625V 0100010: 0.91250V 0100011: 0.91875V 0100100: 0.92500V 0100101: 0.93125V 0100110: 0.93750V

Bit(s)	Mnemonic	Name	Description
			0100111: 0.94375V 0101000: 0.95000V 0101001: 0.95625V 0101010: 0.96250V 0101011: 0.96875V 0101100: 0.97500V 0101101: 0.98125V 0101110: 0.98750V 0101111: 0.99375V 0110000: 1.00000V 0110001: 1.00625V 0110010: 1.01250V 0110011: 1.01875V 0110100: 1.02500V 0110101: 1.03125V 0110110: 1.03750V 0110111: 1.04375V 0111000: 1.05000V 0111001: 1.05625V 0111010: 1.06250V 0111011: 1.06875V 0111100: 1.07500V 0111101: 1.08125V 0111110: 1.08750V 0111111: 1.09375V 1000000: 1.10000V 1000001: 1.10625V 1000010: 1.11250V 1000011: 1.11875V 1000100: 1.12500V 1000101: 1.13125V 1000110: 1.13750V 1000111: 1.14375V 1001000: 1.15000V 1001001: 1.15625V 1001010: 1.16250V 1001011: 1.16875V 1001100: 1.17500V 1001101: 1.18125V 1001110: 1.18750V 1001111: 1.19375V 1010000: 1.20000V 1010001: 1.20625V 1010010: 1.21250V 1010011: 1.21875V 1010100: 1.22500V 1010101: 1.23125V 1010110: 1.23750V 1010111: 1.24375V 1011000: 1.25000V 1011001: 1.25625V 1011010: 1.26250V 1011011: 1.26875V 1011100: 1.27500V 1011101: 1.28125V 1011110: 1.28750V 1011111: 1.29375V 1100000: 1.30000V 1100001: 1.30625V 1100010: 1.31250V 1100011: 1.31875V

Bit(s)	Mnemonic	Name	Description
			1100100: 1.32500V 1100101: 1.33125V 1100110: 1.33750V 1100111: 1.34375V 1101000: 1.35000V 1101001: 1.35625V 1101010: 1.36250V 1101011: 1.36875V 1101100: 1.37500V 1101101: 1.38125V 1101110: 1.38750V 1101111: 1.39375V 1110000: 1.40000V 1110001: 1.40625V 1110010: 1.41250V 1110011: 1.41875V 1110100: 1.42500V 1110101: 1.43125V 1110110: 1.43750V 1110111: 1.44375V 1111000: 1.45000V 1111001: 1.45625V 1111010: 1.46250V 1111011: 1.46875V 1111100: 1.47500V 1111101: 1.48125V 1111110: 1.48750V 1111111: 1.49375V

0314 **VCORE_CON10** **VCORE control register 10** **0048**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VCORE_VOSEL_ON						
Type										RW						
Reset										1	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0	VCORE_VOSEL_ON	VCORE_VOSEL_ON	**VOUT selection in normal mode** 0000000: 0.70000V 0000001: 0.70625V 0000010: 0.71250V 0000011: 0.71875V 0000100: 0.72500V 0000101: 0.73125V 0000110: 0.73750V 0000111: 0.74375V 0001000: 0.75000V 0001001: 0.75625V 0001010: 0.76250V 0001011: 0.76875V 0001100: 0.77500V 0001101: 0.78125V 0001110: 0.78750V 0001111: 0.79375V

Bit(s)	Mnemonic	Name	Description
			0010000: 0.80000V 0010001: 0.80625V 0010010: 0.81250V 0010011: 0.81875V 0010100: 0.82500V 0010101: 0.83125V 0010110: 0.83750V 0010111: 0.84375V 0011000: 0.85000V 0011001: 0.85625V 0011010: 0.86250V 0011011: 0.86875V 0011100: 0.87500V 0011101: 0.88125V 0011110: 0.88750V 0011111: 0.89375V 0100000: 0.90000V 0100001: 0.90625V 0100010: 0.91250V 0100011: 0.91875V 0100100: 0.92500V 0100101: 0.93125V 0100110: 0.93750V 0100111: 0.94375V 0101000: 0.95000V 0101001: 0.95625V 0101010: 0.96250V 0101011: 0.96875V 0101100: 0.97500V 0101101: 0.98125V 0101110: 0.98750V 0101111: 0.99375V 0110000: 1.00000V 0110001: 1.00625V 0110010: 1.01250V 0110011: 1.01875V 0110100: 1.02500V 0110101: 1.03125V 0110110: 1.03750V 0110111: 1.04375V 0111000: 1.05000V 0111001: 1.05625V 0111010: 1.06250V 0111011: 1.06875V 0111100: 1.07500V 0111101: 1.08125V 0111110: 1.08750V 0111111: 1.09375V 1000000: 1.10000V 1000001: 1.10625V 1000010: 1.11250V 1000011: 1.11875V 1000100: 1.12500V 1000101: 1.13125V 1000110: 1.13750V 1000111: 1.14375V 1001000: 1.15000V 1001001: 1.15625V 1001010: 1.16250V 1001011: 1.16875V 1001100: 1.17500V

Bit(s)	Mnemonic	Name	Description
			1001101: 1.18125V 1001110: 1.18750V 1001111: 1.19375V 1010000: 1.20000V 1010001: 1.20625V 1010010: 1.21250V 1010011: 1.21875V 1010100: 1.22500V 1010101: 1.23125V 1010110: 1.23750V 1010111: 1.24375V 1011000: 1.25000V 1011001: 1.25625V 1011010: 1.26250V 1011011: 1.26875V 1011100: 1.27500V 1011101: 1.28125V 1011110: 1.28750V 1011111: 1.29375V 1100000: 1.30000V 1100001: 1.30625V 1100010: 1.31250V 1100011: 1.31875V 1100100: 1.32500V 1100101: 1.33125V 1100110: 1.33750V 1100111: 1.34375V 1101000: 1.35000V 1101001: 1.35625V 1101010: 1.36250V 1101011: 1.36875V 1101100: 1.37500V 1101101: 1.38125V 1101110: 1.38750V 1101111: 1.39375V 1110000: 1.40000V 1110001: 1.40625V 1110010: 1.41250V 1110011: 1.41875V 1110100: 1.42500V 1110101: 1.43125V 1110110: 1.43750V 1110111: 1.44375V 1111000: 1.45000V 1111001: 1.45625V 1111010: 1.46250V 1111011: 1.46875V 1111100: 1.47500V 1111101: 1.48125V 1111110: 1.48750V 1111111: 1.49375V

0316 **VCORE_CON11** **VCORE control register 11** **0048**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VCORE_VOSEL_SLEEP						

0316	VCORE_CON11	VCORE control register 11	0048

Type										RW						
Reset										1	0	0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
6:0	**VCORE_VOSEL_SLEEP**	VCORE_VOSEL_SLEEP	**VOUT selection in sleep mode** 0000000: 0.70000V 0000001: 0.70625V 0000010: 0.71250V 0000011: 0.71875V 0000100: 0.72500V 0000101: 0.73125V 0000110: 0.73750V 0000111: 0.74375V 0001000: 0.75000V 0001001: 0.75625V 0001010: 0.76250V 0001011: 0.76875V 0001100: 0.77500V 0001101: 0.78125V 0001110: 0.78750V 0001111: 0.79375V 0010000: 0.80000V 0010001: 0.80625V 0010010: 0.81250V 0010011: 0.81875V 0010100: 0.82500V 0010101: 0.83125V 0010110: 0.83750V 0010111: 0.84375V 0011000: 0.85000V 0011001: 0.85625V 0011010: 0.86250V 0011011: 0.86875V 0011100: 0.87500V 0011101: 0.88125V 0011110: 0.88750V 0011111: 0.89375V 0100000: 0.90000V 0100001: 0.90625V 0100010: 0.91250V 0100011: 0.91875V 0100100: 0.92500V 0100101: 0.93125V 0100110: 0.93750V 0100111: 0.94375V 0101000: 0.95000V 0101001: 0.95625V 0101010: 0.96250V 0101011: 0.96875V 0101100: 0.97500V 0101101: 0.98125V 0101110: 0.98750V 0101111: 0.99375V 0110000: 1.00000V 0110001: 1.00625V 0110010: 1.01250V 0110011: 1.01875V

Bit(s)	Mnemonic	Name	Description
			0110100: 1.02500V 0110101: 1.03125V 0110110: 1.03750V 0110111: 1.04375V 0111000: 1.05000V 0111001: 1.05625V 0111010: 1.06250V 0111011: 1.06875V 0111100: 1.07500V 0111101: 1.08125V 0111110: 1.08750V 0111111: 1.09375V 1000000: 1.10000V 1000001: 1.10625V 1000010: 1.11250V 1000011: 1.11875V 1000100: 1.12500V 1000101: 1.13125V 1000110: 1.13750V 1000111: 1.14375V 1001000: 1.15000V 1001001: 1.15625V 1001010: 1.16250V 1001011: 1.16875V 1001100: 1.17500V 1001101: 1.18125V 1001110: 1.18750V 1001111: 1.19375V 1010000: 1.20000V 1010001: 1.20625V 1010010: 1.21250V 1010011: 1.21875V 1010100: 1.22500V 1010101: 1.23125V 1010110: 1.23750V 1010111: 1.24375V 1011000: 1.25000V 1011001: 1.25625V 1011010: 1.26250V 1011011: 1.26875V 1011100: 1.27500V 1011101: 1.28125V 1011110: 1.28750V 1011111: 1.29375V 1100000: 1.30000V 1100001: 1.30625V 1100010: 1.31250V 1100011: 1.31875V 1100100: 1.32500V 1100101: 1.33125V 1100110: 1.33750V 1100111: 1.34375V 1101000: 1.35000V 1101001: 1.35625V 1101010: 1.36250V 1101011: 1.36875V 1101100: 1.37500V 1101101: 1.38125V 1101110: 1.38750V 1101111: 1.39375V 1110000: 1.40000V

Bit(s)	Mnemonic	Name	Description
			1110001: 1.40625V 1110010: 1.41250V 1110011: 1.41875V 1110100: 1.42500V 1110101: 1.43125V 1110110: 1.43750V 1110111: 1.44375V 1111000: 1.45000V 1111001: 1.45625V 1111010: 1.46250V 1111011: 1.46875V 1111100: 1.47500V 1111101: 1.48125V 1111110: 1.48750V 1111111: 1.49375V

0318 **VCORE_CON12** **VCORE control register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										NI_VCORE_VOSEL						
Type										RO						
Reset										0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
			VOUT selection
6:0	**NI_VCORE_VOSEL**	NI_VCORE_VOSEL	0000000: 0.70000V 0000001: 0.70625V 0000010: 0.71250V 0000011: 0.71875V 0000100: 0.72500V 0000101: 0.73125V 0000110: 0.73750V 0000111: 0.74375V 0001000: 0.75000V 0001001: 0.75625V 0001010: 0.76250V 0001011: 0.76875V 0001100: 0.77500V 0001101: 0.78125V 0001110: 0.78750V 0001111: 0.79375V 0010000: 0.80000V 0010001: 0.80625V 0010010: 0.81250V 0010011: 0.81875V 0010100: 0.82500V 0010101: 0.83125V 0010110: 0.83750V 0010111: 0.84375V 0011000: 0.85000V 0011001: 0.85625V 0011010: 0.86250V 0011011: 0.86875V 0011100: 0.87500V

Bit(s)	Mnemonic	Name	Description
			0011101: 0.88125V 0011110: 0.88750V 0011111: 0.89375V 0100000: 0.90000V 0100001: 0.90625V 0100010: 0.91250V 0100011: 0.91875V 0100100: 0.92500V 0100101: 0.93125V 0100110: 0.93750V 0100111: 0.94375V 0101000: 0.95000V 0101001: 0.95625V 0101010: 0.96250V 0101011: 0.96875V 0101100: 0.97500V 0101101: 0.98125V 0101110: 0.98750V 0101111: 0.99375V 0110000: 1.00000V 0110001: 1.00625V 0110010: 1.01250V 0110011: 1.01875V 0110100: 1.02500V 0110101: 1.03125V 0110110: 1.03750V 0110111: 1.04375V 0111000: 1.05000V 0111001: 1.05625V 0111010: 1.06250V 0111011: 1.06875V 0111100: 1.07500V 0111101: 1.08125V 0111110: 1.08750V 0111111: 1.09375V 1000000: 1.10000V 1000001: 1.10625V 1000010: 1.11250V 1000011: 1.11875V 1000100: 1.12500V 1000101: 1.13125V 1000110: 1.13750V 1000111: 1.14375V 1001000: 1.15000V 1001001: 1.15625V 1001010: 1.16250V 1001011: 1.16875V 1001100: 1.17500V 1001101: 1.18125V 1001110: 1.18750V 1001111: 1.19375V 1010000: 1.20000V 1010001: 1.20625V 1010010: 1.21250V 1010011: 1.21875V 1010100: 1.22500V 1010101: 1.23125V 1010110: 1.23750V 1010111: 1.24375V 1011000: 1.25000V 1011001: 1.25625V

Bit(s)	Mnemonic	Name	Description
			1011010: 1.26250V 1011011: 1.26875V 1011100: 1.27500V 1011101: 1.28125V 1011110: 1.28750V 1011111: 1.29375V 1100000: 1.30000V 1100001: 1.30625V 1100010: 1.31250V 1100011: 1.31875V 1100100: 1.32500V 1100101: 1.33125V 1100110: 1.33750V 1100111: 1.34375V 1101000: 1.35000V 1101001: 1.35625V 1101010: 1.36250V 1101011: 1.36875V 1101100: 1.37500V 1101101: 1.38125V 1101110: 1.38750V 1101111: 1.39375V 1110000: 1.40000V 1110001: 1.40625V 1110010: 1.41250V 1110011: 1.41875V 1110100: 1.42500V 1110101: 1.43125V 1110110: 1.43750V 1110111: 1.44375V 1111000: 1.45000V 1111001: 1.45625V 1111010: 1.46250V 1111011: 1.46875V 1111100: 1.47500V 1111101: 1.48125V 1111110: 1.48750V 1111111: 1.49375V

0402 **ANALDO_CON1** **Analog LDO control register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VTCXO_EN								DA_QI_VTCXO_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Mnemonic	Name	Description
15	**DA_QI_**	DA_QI_VTCXO_	**VXO22 qi_enable which is an output signal connected to**

Bit(s)	Mnemonic	Name	Description
	VTCXO_EN	EN	analog model directly
7	DA_QI_VTCXO_MODE	DA_QI_VTCXO_MODE	VXO22 low power mode output

0404 **ANALDO_CON2** **Analog LDO control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VAUD22_EN								DA_QI_VAUD22_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Mnemonic	Name	Description
15	DA_QI_VAUD22_EN	DA_QI_VAUD22_EN	vaud22 qi_enable
7	DA_QI_VAUD22_MODE	DA_QI_VAUD22_MODE	vaud22 low power mode

0408 **ANALDO_CON4** **Analog LDO control register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VCAMA_EN															
Type	RW															
Reset	0															

Bit(s)	Mnemonic	Name	Description
15	RG_VCAMA_EN	RG_VCAMA_EN	VCAMA enable when choosing sw ctrl 1'b1: enable 1'b0: disable

0412 **ANALDO_CON10** **Analog LDO control register 10** **0060**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RG_VCAMA_VOSEL											
Type					RW											
Reset					0	0	0	0	0	1	1					

Bit(s)	Mnemonic	Name	Description
11:5	RG_VCAMA_VOSEL	RG_VCAMA_VOSEL	output voltage select 2'b00: 1.5 v 2'b01: 1.8 v 2'b10: 2.5 v 2'b11: 2.8 v

0420 **ANALDO_CON21** **Analog LDO control register 21** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DA_QI_VCN35_MODE							
Type									RO							
Reset									0							

Bit(s)	Mnemonic	Name	Description
7	DA_QI_VCN35_MODE	DA_QI_VCN35_MODE	low power mode enable (shouldn't use PMU_RSTB to gate D/A interface LS) 0: normal mode 1: low power mode 0: normal mode 1: low power mode

0424 **ANALDO_CON23** **Analog LDO control register 23** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VAUD28_EN								DA_QI_VAUD28_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Mnemonic	Name	Description
15	**DA_QI_VAUD28_EN**	DA_QI_VAUD28_EN	**qi_enable**
7	**DA_QI_VAUD28_MODE**	DA_QI_VAUD28_MODE	**low power mode enable (shouldn't use PMU_RSTB to gate D/A interface LS)** 0: normal mode 1: low power mode

0428 **ANALDO_CON25** **Analog LDO control register 25** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VADC18_EN								DA_QI_VADC18_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Mnemonic	Name	Description
15	**DA_QI_VADC18_EN**	DA_QI_VADC18_EN	**qi_enable**
7	**DA_QI_VADC18_MODE**	DA_QI_VADC18_MODE	**low power mode enable (shouldn't use PMU_RSTB to gate D/A interface LS)** 0: normal mode 1: low power mode

042E **ANALDO_CON28** **Analog LDO control register 28** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RGS_QI_VTCXO_OC_STATUS_DEBOUNCE	RGS_QI_VADC18_OC_STATUS_DEBOUNCE	RGS_QI_VAUD22_OC_STATUS_DEBOUNCE	RGS_QI_VAUD28_OC_STATUS_DEBOUNCE	RGS_QI_VCAMA_OC_STATUS_DEBOUNCE											
Type	RO	RO	RO	RO	RO											
Reset	0	0	0	0	0											

Bit(s)	Mnemonic	Name	Description
15	**RGS_QI_VTCXO_OC_STATUS_DEBOUNCE**	RGS_QI_VTCXO_OC_STATUS_DEBOUNCE	**over current status** 1'b1: over current occur 1'b0: no over current occur
14	**RGS_QI_VADC18_OC_STATUS_DEBOUNCE**	RGS_QI_VADC18_OC_STATUS_DEBOUNCE	**over current status** 1'b1: over current occur 1'b0: no over current occur
13	**RGS_QI_VAUD22_OC_STATUS_DEBOUNCE**	RGS_QI_VAUD22_OC_STATUS_DEBOUNCE	**over current status** 1'b1: over current occur 1'b0: no over current occur
12	**RGS_QI_VAUD28_OC_STATUS_DEBOUNCE**	RGS_QI_VAUD28_OC_STATUS_DEBOUNCE	**over current status** 1'b1: over current occur 1'b0: no over current occur
11	**RGS_QI_VCAMA_OC_STATUS_DEBOUNCE**	RGS_QI_VCAMA_OC_STATUS_DEBOUNCE	**over current status** 1'b1: over current occur 1'b0: no over current occur

0500 **DIGLDO_CON0** **Digital LDO control register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DA_QI_VIO28_EN**								**DA_QI_VIO28_MODE**							
Type	RO								RO							
Reset	0								0							

Bit(s)	Name	Description
15	DA_QI_VIO28_EN	**quiescent enable to analog interface**
7	DA_QI_VIO28_MODE	**low power mode indicator to analog input**

0502 **DIGLDO_CON2** **Digital LDO control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

0502 **DIGLDO_CON2** **Digital LDO control register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VUSB_EN								DA_QI_VUSB_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Name	Description
15	DA_QI_VUSB_EN	**quiescent enable to analog interface**
7	DA_QI_VUSB_MODE	**low power mode indicator to analog input**

0504 **DIGLDO_CON3** **Digital LDO control register 3** **1000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VMC_EN			RG_VMC_EN					DA_QI_VMC_MODE							
Type	RO			RW					RO							
Reset	0			1					0							

Bit(s)	Name	Description
15	DA_QI_VMC_EN	**quiescent enable to analog interface**
12	RG_VMC_EN	**VMC register enable input**
7	DA_QI_VMC_MODE	**low power mode indicator to analog input**

0506 **DIGLDO_CON5** **Digital LDO control register 5** **4000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VMCH_EN	RG_VMCH_EN							DA_QI_VMCH_MODE							
Type	RO	RW							RO							
Reset	0	1							0							

Bit(s)	Name	Description
15	DA_QI_VMCH_EN	**quiescent enable to analog interface**

Bit(s)	Name	Description
14	RG_VMCH_EN	**VMCH register enable input**
7	DA_QI_VMCH_MODE	**low power mode indicator to analog input**

0508 **DIGLDO_CON6** **Digital LDO control register 6** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VEMC_3V3_EN								DA_QI_VEMC_3V3_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Name	Description
15	DA_QI_VEMC_3V3_EN	**quiescent enable to analog interface**
7	DA_QI_VEMC_3V3_MODE	**low power mode indicator to analog input**

050A **DIGLDO_CON7** **Digital LDO control register 7** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VGP1_EN								DA_QI_VGP1_MODE							
Type	RW								RO							
Reset	0								0							

Bit(s)	Name	Description
15	RG_VGP1_EN	**VGP1 soft Enable**
7	DA_QI_VGP1_MODE	**low power mode indicator to analog input**

050C **DIGLDO_CON8** **Digital LDO control register 8** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_V								DA_QI							

050C **DIGLDO_CON8** **Digital LDO control register 8** **0000**

	GP2_EN								_VGP2_MODE							
Type	RW								RO							
Reset	0								0							

Bit(s)	Name	Description
15	RG_VGP2_EN	VGP2 soft Enable
7	DA_QI_VGP2_MODE	low power mode indicator to analog input

0512 **DIGLDO_CON11** **Digital LDO control register 11** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCN_1V8_EN								DA_QI_VCN_1V8_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Name	Description
15	DA_QI_VCN_1V8_EN	quiescent enable to analog interface
7	DA_QI_VCN_1V8_MODE	low power mode indicator to analog input

051A **DIGLDO_CON15** **Digital LDO control register 15** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VRTC_EN															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	DA_QI_VRTC_EN	quiescent enable to analog interface

052A **DIGLDO_CON24** **Digital LDO control register 24** 0010

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												RG_VMC_VOSEL				
Type												RW				
Reset												1				

Bit(s)	Name	Description
4	RG_VMC_VOSEL	**output selection signal** (1'b1 : 3.3 V) 1'b0 : 1.8 V 1'b1 : 3.3 V

052C **DIGLDO_CON26** **Digital LDO control register 26** 0080

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VMCH_VOSEL							
Type									RW							
Reset									1							

Bit(s)	Name	Description
7	RG_VMCH_VOSEL	**output selection signal** (1'b1 : 3.3 V) 1'b0 : 3.0 V 1'b1 : 3.3 V

0530 **DIGLDO_CON28** **Digital LDO control register 28** 00A0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VGP1_VOSEL							
Type									RW							
Reset									1	0	1					

Bit(s)	Name	Description
7:5	RG_VGP1_VOSEL	**output selection signal** (3'b101: 2.8 V) 3'b000: 1.2 V 3'b001: 1.3 V 3'b010: 1.5 V

Bit(s)	Name	Description
		3'b011: 1.8 V 3'b100: 2.0 V 3'b101: 2.8 V 3'b110: 3.0 V 3'b111: 3.3 V

0532 **DIGLDO_CON29** **Digital LDO control register 29** **00A0**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VGP2_VOSEL							
Type									RW							
Reset									1	0	1					

Bit(s)	Name	Description
7:5	RG_VGP2_VOSEL	**output selection signal** (3'b101: 2.8 V) 3'b000: 1.2 V 3'b001: 1.3 V 3'b010: 1.5 V 3'b011: 1.8 V 3'b100: 2.0 V 3'b101: 2.8 V 3'b110: 3.0 V 3'b111: 3.3 V

0536 **DIGLDO_CON31** **Digital LDO control register 31** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RG_VCAM_AF_EN								DA_QI_VCAM_AF_MODE							
Type	RW								RO							
Reset	0								0							

Bit(s)	Name	Description
15	RG_VCAM_AF_EN	**vcam_af register Enable input**
7	DA_QI_VCAM_AF_MODE	**low power mode indicator to analog input**

0538 **DIGLDO_CON32** **Digital LDO control register 32** **0080**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

0538 **DIGLDO_CON32** **Digital LDO control register 32** **0080**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RG_VCAM_AF_VOSEL							
Type									RW							
Reset									1	0	0					

Bit(s)	Name	Description
7:5	RG_VCAM_AF_VOSEL	**output selection signal** (3'b100 : 2.0 V) 3'b000 : 1.2 V 3'b001 : 1.3 V 3'b010 : 1.5 V 3'b011 : 1.8 V 3'b100 : 2.0 V 3'b101 : 2.8 V 3'b110 : 3.0 V 3'b111 : 3.3 V

0552 **DIGLDO_CON47** **Digital LDO control register 47** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VM_EN								DA_QI_VM_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Name	Description
15	DA_QI_VM_EN	**quiescent enable to analog interface**
7	DA_QI_VM_MODE	**low power mode indicator to analog input**

0556 **DIGLDO_CON49** **Digital LDO control register 49** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VIO18_EN								DA_QI_VIO18_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Name	Description
15	DA_QI_VIO18_EN	**quiescent enable to analog interface**
7	DA_QI_VIO18_MO	**low power mode indicator to analog input**

Bit(s)	Name	Description
	DE	

055A **DIGLDO_CON51** **Digital LDO control register 51** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCAMD_EN	RG_VCAMD_EN							DA_QI_VCAMD_MODE							
Type	RO	RW							RO							
Reset	0	0							0							

Bit(s)	Name	Description
15	DA_QI_VCAMD_EN	**quiescent enable to analog interface**
14	RG_VCAMD_EN	**vcamd register enable input**
7	DA_QI_VCAMD_MODE	**low power mode indicator to analog input**

055C **DIGLDO_CON52** **Digital LDO control register 52** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_VCAMD_VOSEL						
Type										RW						
Reset										0	0					

Bit(s)	Name	Description
6:5	RG_VCAMD_VOSEL	**output selection signal** (2'b00: 1.2 V) 2'b00: 1.2 V 2'b01: 1.3 V 2'b10: 1.5 V 2'b11: 1.8 V

055E **DIGLDO_CON53** **Digital LDO control register 53** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VCAM_IO	RG_VCAM_IO_E							DA_QI_VCAM_IO_							

055E **DIGLDO_CON53** **Digital LDO control register 53** **0000**

	_EN	N							MODE							
Type	RO	RW							RO							
Reset	0	0							0							

Bit(s)	Name	Description
15	DA_QI_VCAM_IO_EN	quiescent enable to analog interface
14	RG_VCAM_IO_EN	vcam_io enable
7	DA_QI_VCAM_IO_MODE	low power mode indicator to analog input

0562 **DIGLDO_CON55** **Digital LDO control register 55** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VM25_EN								DA_QI_VM25_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Name	Description
15	DA_QI_VM25_EN	quiescent enable to analog interface
7	DA_QI_VM25_MODE	low power mode indicator to analog input

0566 **DIGLDO_CON57** **Digital LDO control register 57** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DA_QI_VEFUSE_EN								DA_QI_VEFUSE_MODE							
Type	RO								RO							
Reset	0								0							

Bit(s)	Name	Description
15	DA_QI_VEFUSE_EN	quiescent enable to analog interface
7	DA_QI_VEFUSE_M	low power mode indicator to analog input

Bit(s)	Name	Description
	ODE	

0570	DIGLDO_CON62	Digital LDO control register 62	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RGS_QI_VCN35_OC_STATUS_DEBOUNCE	RGS_QI_VIO28_OC_STATUS_DEBOUNCE	RGS_QI_VUSB_OC_STATUS_DEBOUNCE	RGS_QI_VMC_OC_STATUS_DEBOUNCE	RGS_QI_VMCH_OC_STATUS_DEBOUNCE	RGS_QI_VEMC_3V3_OC_STATUS_DEBOUNCE	RGS_QI_VCAM_AF_OC_STATUS_DEBOUNCE	RGS_QI_VGP1_OC_STATUS_DEBOUNCE	RGS_QI_VGP2_OC_STATUS_DEBOUNCE	RGS_QI_VM25_OC_STATUS_DEBOUNCE	RGS_QI_VEFUSE_OC_STATUS_DEBOUNCE	RGS_QI_VM_OC_STATUS_DEBOUNCE	RGS_QI_VIO18_OC_STATUS_DEBOUNCE	RGS_QI_VCN_1V8_OC_STATUS_DEBOUNCE	RGS_QI_VCAMD_OC_STATUS_DEBOUNCE	RGS_QI_VCAM_IO_OC_STATUS_DEBOUNCE
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	RGS_QI_VCN35_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
14	RGS_QI_VIO28_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
13	RGS_QI_VUSB_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
12	RGS_QI_VMC_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
11	RGS_QI_VMCH_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
10	RGS_QI_VEMC_3V3_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
9	RGS_QI_VCAM_AF_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
8	RGS_QI_VGP1_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
7	RGS_QI_VGP2_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
6	RGS_QI_VM25_OC_STATUS_DEBOU	**1'b1: over current occur**

Bit(s)	Name	Description
	NCE	1'b0: no over current occur
5	RGS_QI_VEFUSE_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
4	RGS_QI_VM_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
3	RGS_QI_VIO18_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
2	RGS_QI_VCN_1V8_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
1	RGS_QI_VCAMD_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur
0	RGS_QI_VCAM_IO_OC_STATUS_DEBOUNCE	**1'b1: over current occur** 1'b0: no over current occur

0700 **AUXADC_ADC0** **AUXADC ADC register 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH0	AUXADC_ADC_OUT_CH0														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH0	**AUXADC channel 0 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH0	**AUXADC channel 0 output data**

0702 **AUXADC_ADC1** **AUXADC ADC register 1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY	AUXADC_ADC_OUT_CH1														

0702 **AUXADC_ADC1** **AUXADC ADC register 1** **0000**

	_CH1															
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH1	**AUXADC channel 1 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH1	**AUXADC channel 1 output data**

0704 **AUXADC_ADC2** **AUXADC ADC register 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH2				AUXADC_ADC_OUT_CH2											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH2	**AUXADC channel 2 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH2	**AUXADC channel 2 output data**

0706 **AUXADC_ADC3** **AUXADC ADC register 3** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH3				AUXADC_ADC_OUT_CH3											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH3	**AUXADC channel 3 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH3	**AUXADC channel 3 output data**

0708 **AUXADC_ADC4** **AUXADC ADC register 4** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH4				AUXADC_ADC_OUT_CH4											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH4	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH4	**AUXADC channel 4 output data**

070A **AUXADC_ADC5** **AUXADC ADC register 5** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH5				AUXADC_ADC_OUT_CH5											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH5	**AUXADC channel 5 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH5	**AUXADC channel 5 output data**

070C	AUXADC_ADC6	AUXADC ADC register 6	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH6				AUXADC_ADC_OUT_CH6											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH6	**AUXADC channel 6 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH6	**AUXADC channel 6 output data**

070E	AUXADC_ADC7	AUXADC ADC register 7	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH7	AUXADC_ADC_OUT_CH7														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH7	**AUXADC channel 7 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_CH7	**AUXADC channel 7 output data**

0710	AUXADC_ADC8	AUXADC ADC register 8	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_R				AUXADC_ADC_OUT_CH8											

0710 **AUXADC_ADC8** **AUXADC ADC register 8** 0000

	DY_CH8															
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH8	**AUXADC channel 8 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH8	**AUXADC channel 8 output data**

0712 **AUXADC_ADC9** **AUXADC ADC register 9** 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH9				AUXADC_ADC_OUT_CH9											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH9	**AUXADC channel 9 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH9	**AUXADC channel 9 output data**

0714 **AUXADC_ADC10** **AUXADC ADC register 10** 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH10				AUXADC_ADC_OUT_CH10											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH10	**AUXADC channel 10 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH10	**AUXADC channel 10 output data**

0716 **AUXADC_ADC11** **AUXADC ADC register 11** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH11				AUXADC_ADC_OUT_CH11											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH11	**AUXADC channel 11 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH11	**AUXADC channel 11 output data**

0718 **AUXADC_ADC12** **AUXADC ADC register 12** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_CH12_15				AUXADC_ADC_OUT_CH12_15											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_CH12_15	**AUXADC channel 12_15 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_CH12_15	**AUXADC channel 12_15 output data**

071A	AUXADC_ADC13	AUXADC ADC register 13	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_THR_HW				AUXADC_ADC_OUT_THR_HW											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_THR_HW	**AUXADC channel 4 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_THR_HW	**AUXADC channel 4 output data**

071C	AUXADC_ADC14	AUXADC ADC register 14	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_LBAT				AUXADC_ADC_OUT_LBAT											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_LBAT	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_LBAT	**AUXADC low battery output data**

071E	AUXADC_ADC15	AUXADC ADC register 15	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

071E **AUXADC_ADC15** **AUXADC ADC register 15** 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_WAKEUP_PCHR	AUXADC_ADC_OUT_WAKEUP_PCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_PCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_PCHR	**AUXADC wakeup output data**

0720 **AUXADC_ADC16** **AUXADC ADC register 16** 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_WAKEUP_SWCHR	AUXADC_ADC_OUT_WAKEUP_SWCHR														
Type	RO	RO														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_WAKEUP_SWCHR	**AUXADC wakeup output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
14:0	AUXADC_ADC_OUT_WAKEUP_SWCHR	**AUXADC wakeup output data**

0726	AUXADC_ADC19	AUXADC ADC register 19	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AUXADC_ADC_OUT_RAW														
Type		RO														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
14:0	AUXADC_ADC_OUT_RAW	**AUXADC channel output raw data**

072A	AUXADC_ADC21	AUXADC ADC register 21	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_TYPEC_H				AUXADC_ADC_OUT_TYPEC_H											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_TYPEC_H	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_TYPEC_H	**AUXADC low battery output data**

072C	AUXADC_ADC22	AUXADC ADC register 22	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_RDY_TYPEC_L				AUXADC_ADC_OUT_TYPEC_L											
Type	RO				RO											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_RDY_TYPEC_L	**AUXADC low battery output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
11:0	AUXADC_ADC_OUT_TYPEC_L	**AUXADC low battery output data**

072E **AUXADC_STA0** **AUXADC_STA0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUXADC_ADC_BUSY_IN_WAKEUP			AUXADC_ADC_BUSY_IN_LBAT	AUXADC_ADC_BUSY_IN											
Type	RO			RO	RO											
Reset	0			0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	AUXADC_ADC_BUSY_IN_WAKEUP	**ADC busy status** 1: BUSY 0: IDLE
12	AUXADC_ADC_BUSY_IN_LBAT	**ADC busy status** 1: BUSY 0: IDLE
11:0	AUXADC_ADC_BUSY_IN	**AUXADC ADC BUSY STATUS, bit[11] = CH11 ~ bit[0] = CH0** 1 : BUSY 0 : IDLE

0730 **AUXADC_STA1** **AUXADC_STA1** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		AUXADC_ADC_BUSY_IN_THR_HW	AUXADC_ADC_BUSY_IN_SHARE		AUXADC_ADC_BUSY_IN_TYPEC_L	AUXADC_ADC_BUSY_IN_TYPEC_H										
Type		RO	RO		RO	RO										
Reset		0	0		0	0										

Bit(s)	Name	Description
14	AUXADC_ADC_BUSY_IN_THR_HW	**ADC busy status** 1: BUSY 0: IDLE
13	AUXADC_ADC_BUSY_IN_SHARE	**ADC busy status** 1: BUSY 0: IDLE
11	AUXADC_ADC_BUSY_IN_TYPEC_L	**ADC busy status** 1: BUSY 0: IDLE
10	AUXADC_ADC_BUSY_IN_TYPEC_H	**ADC busy status** 1: BUSY 0: IDLE

0800 **TYPE_C_PHY_RG_0** **TYPE-C PHY RG 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															type_c_phy_rg_cc_rp_sel	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	type_c_phy_rg_cc_rp_sel	**Type-C PHY RG RP selection of default USB power or 1.5A or 3A** 00: 36K ohm, default USB power 01: 12K ohm, 1.5A 10: 4.7K ohm, 3A 11: reserved Default Value: 2'b00 [NORMAL] 2'b00 [SCAN] 2'b00 [OLT]

0806 **TYPE_C_CTRL** **TYPE-C Control** **0800**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reg_type_c_try_wait_src2attach_src_deb_sel	reg_type_c_da_cc_sacl k_sw_en	reg_type_c_disable_st_rd_en			reg_type_c_attach_src_2_try_wait_snk_st_en	reg_type_c_try_snk_st_en	reg_type_c_try_src_st_en	reg_type_c_debug_acc_en	reg_type_c_audio_acc_en	reg_type_c_acc_en	reg_type_c_adc_en	reg_type_c_port_support_role	
Type			RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	

0806	TYPE_C_CTRL	TYPE-C Control	0800

Reset			0	0	1			0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	reg_type_c_try_wait_src2attach_src_deb_sel	**TryWait.SRC to Attach.SRC deounce select. Select use tPDDebounce or tPDDebounce** 1'b0: tPDDebounce 1'b1: tCCDebounce
12	reg_type_c_da_cc_saclk_sw_en	**DA_SACLK software enable** 1'b0: Disable. Clock enable is control by HW. 1'b1: Enable. Clcock is on.
11	reg_type_c_disable_st_rd_en	**Disable state Rd termination enable** 1'b0: Disable. Disable state do not has any terminatiion. 1'b1: Enable. Disable state has Rd terminatiion.
8	reg_type_c_attach_src_2_try_wait_snk_st_en	**Attach.SRC to TryWait.SNK state enable** 1'b0: Disable 1'b1: Enable. Enable Try Attach.SRC to TryWait.SNK state transition.
7	reg_type_c_try_snk_st_en	**Try Sink state enable** 1'b0: Disable 1'b1: Enable. Enable Try,SNK state. Try.SRC & Try.SNK can not be suppoorted at the same time.
6	reg_type_c_try_src_st_en	**Try Source state enable** 1'b0: Disable 1'b1: Enable. Enable Try.SRC state. Try.SRC & Try.SNK can not be suppoorted at the same time.
5	reg_type_c_debug_acc_en	**Debug accessory mode enable.** 1'b0: Disable 1'b1: Enable. Support Debug accessory mode. Both DebugAccessorySRC & DebugAccessorySNK.
4	reg_type_c_audio_acc_en	**Audio accessory mode enable.** 1'b0: Disable 1'b1: Enable. Support Audio accessory mode.
3	reg_type_c_acc_en	**Accessory mode enable.** 1'b0: Disable 1'b1: Enable. Support Accessory mode.
2	reg_type_c_adc_en	**ADC use enable.** 1'b0: Disable 1;b1: Enable. Use ADC detect Rp change in Atrtach.SNK state
1:0	reg_type_c_port_support_role	**Port support role.** 2'b00: Sink 2:b01: Source 2'b10: DRP 2'b11: Reserved

080A	TYPE_C_CC_SW_CTRL	TYPE-C CC Stoftware Control	0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	wi_type_						type_cc_s	type_cc_s						wi_type_	wi_type_	wi_type_

080A **TYPE_C_CC_SW_CTRL** **TYPE-C CC Stoftware Control** **0000**

	c_sw_ent_snk_pwr_redetect_cmd						w_da_drive_vconn_en	w_vbus_present						c_sw_ent_unatch_snk_cmd	c_sw_ent_unatch_src_cmd	c_sw_ent_disable_cmd
Type	WO						Ao	RW						WO	WO	WO
Reset	0						0	0						0	0	0

Bit(s)	Name	Description
15	w1_type_c_sw_ent_snk_pwr_redetect_cmd	**Type-C software enter Sink power redetect state command. Valid when Sink power sub-state not in Idle state.**
9	type_c_sw_da_drive_vconn_en	**Type-C software drive VCONN enable** 1'b0: Disable 1'b1: Enable
8	type_c_sw_vbus_present	**Type-C software VBUS present.** 0: VBUS not present 1: VBUS present
2	w1_type_c_sw_ent_unatch_snk_cmd	**Type-C software enter unatach Sink state command**
1	w1_type_c_sw_ent_unatch_src_cmd	**Type-C software enter unatach Source state command**
0	w1_type_c_sw_ent_disable_cmd	**Type-C software enter disable state command**

080C **TYPE_C_CC_VOL_PERIODIC_MEAS_VAL** **TYPE-C CC Voltage Periodic Measure Value** **02ED**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**reg_type_c_cc_vol_periodic_meas_val**												
Type				RW												
Reset				0	0	0	1	0	1	1	1	0	1	1	0	1

Bit(s)	Name	Description
12:0	reg_type_c_cc_vol_periodic_meas_val	**Type-C CC voltage periodic measure value** Every (periodic measure value) cycle counts will trigger one voltage measure event. Not to over 15ms. 15ms is the minimum time tha DRP stay in certain unattach state. Not to smaller than 1ms. Make sure to measure stable voltage after cc termination is changed. Default set 10ms. Suppose cc_ck is 75KHz. type_c_cc_vol_periodic_meas_val default value is (750 -1).

Bit(s)	Name	Description
		Suggest using 5ms which is the safest settings. If cc_ck is 75KHz, set value to (375-1).

080E **TYPE_C_CC_VOL_DEBOUCE_CNT_VAL** **TYPE-C CC Voltage Debounce Count Value** **020A**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				reg_type_c_cc_vol_pd_debounce_cnt_val					reg_type_c_cc_vol_cc_debounce_cnt_val							
Type				RW					RW							
Reset				0	0	0	1	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
12:8	reg_type_c_cc_vol_pd_debounce_cnt_val	**Type-C CC Voltage PD debounce count value** PD deounce time met when voltage measurement result is the same for PD debounce counts. tCCDebounce: 10ms ~ 20ms Set value = (tPDDebounce/(type_c_cc_vcomp_periodic_meas_val +1)) Use 20ms & suppose measure period is 10ms. Default set to 2 Suggest using 15ms which is the safest settings. Set value to 3.
7:0	reg_type_c_cc_vol_cc_debounce_cnt_val	**Type-C CC Voltage CC debounce count value** CC deounce time met when voltage measurement result is the same for CC debounce counts. tCCDebounce: 100ms ~ 200ms Set value = (tCCDebounce/(type_c_cc_vcomp_periodic_meas_val+1) Use 100ms & suppose measure period is 10ms. Default set to 10 Suggest using 150ms which is the safest settings. Set value to 30.

0810 **TYPE_C_DRP_SRC_CNT_VAL_0** **TYPE-C DRP Source Count Value 0** **0EA5**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_type_c_drp_src_cnt_val_0															
Type	RW															
Reset	0	0	0	0	1	1	1	0	1	0	1	0	0	1	0	1

Bit(s)	Name	Description
15:0	reg_type_c_drp_src_cnt_val_0	**Type-C DRP Source count value 0** The time that DRP stay in Unattached.SRC state. Indicate type_c_drp_src_cnt_val[15:0] Default set 50ms. Suppose cc_ck is 75KHz. type_c_cc_vol_periodic_meas_val default value is (3750 -1). Suggest using 37.5ms which is the safest settings. If cc_ck is 75KHz, set value to 2812.

0814 **TYPE_C_DRP_SNK_CNT_VAL_0** **TYPE-C DRP Sink Count Value 0** **0EA5**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_type_c_drp_snk_cnt_val_0															
Type	RW															
Reset	0	0	0	0	1	1	1	0	1	0	1	0	0	1	0	1

Bit(s)	Name	Description
15:0	reg_type_c_drp_snk_cnt_val_0	**Type-C DRP Sink count value 0** The time that DRP stay in Unattached.SNK state. Indicate type_c_drp_snk_cnt_val[15:0] Spec 50~100ms Default use 50ms Suppose cc_ck is 75KHz. type_c_cc_vol_periodic_meas_val default value is (3750 -1). Suggest using 37.5ms which is the safest settings. If cc_ck is 75KHz, set value to 2812.

0818 **TYPE_C_DRP_TRY_CNT_VAL_0** **TYPE-C DRP Try Count Value 0** **1D4B**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_type_c_drp_try_cnt_val_0															
Type	RW															
Reset	0	0	0	1	1	1	0	1	0	1	0	0	1	0	1	1

Bit(s)	Name	Description
15:0	reg_type_c_drp_try_cnt_val_0	**Type-C DRP Try count value 0** The time that DRP stay in Try.SRC state. Indicate type_c_drp_try_cnt_val[15:0] Spec 75~150ms Default use 100ms Suppose cc_ck is 75KHz. type_c_cc_vol_periodic_meas_val default value is (7500 -1). Suggest using 112.5ms which is the safest settings. If cc_ck is 75KHz, set value to 8437.

0820 **TYPE_C_CC_SRC_DEFAULT_DAC_VAL** **TYPE-C CC SRC Default DAC Value** **0225**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reg_type_c_cc_src_vrd_default_dac_val								reg_type_c_cc_src_vopen_default_dac_val					
Type			RW								RW					
Reset			0	0	0	0	1	0			1	0	0	1	0	1

Bit(s)	Name	Description
13:8	reg_type_c_cc_src_vrd_default_dac_val	**Type-C CC Source VRD default DAC value** The value to for DAC to compare Source VRD voltage when support default current
5:0	reg_type_c_cc_src_vopen_default_dac_val	**Type-C CC Source VOPEN default DAC value** The value to for DAC to compare Source VOPEN voltage when support default current

0822 **TYPE_C_CC_SRC_15_DAC_VAL** **TYPE-C CC SRC 15 DAC Value** **0725**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reg_type_c_cc_src_vrd_15_dac_val								reg_type_c_cc_src_vopen_15_dac_val					
Type			RW								RW					
Reset			0	0	0	1	1	1			1	0	0	1	0	1

Bit(s)	Name	Description
13:8	reg_type_c_cc_src_vrd_15_dac_val	**Type-C CC Source VRD 15 DAC value** The value to for DAC to compare Source VRD voltage when support 1.5A current
5:0	reg_type_c_cc_src_vopen_15_dac_val	**Type-C CC Source VOPEN 15 DAC value** The value to for DAC to compare Source VOPEN voltage when support 1.5A current

0824 **TYPE_C_CC_SRC_30_DAC_VAL** **TYPE-C CC SRC 30 DAC Value** **113E**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reg_type_c_cc_src_vrd_30_dac_val								reg_type_c_cc_src_vopen_30_dac_val					
Type			RW								RW					
Reset			0	1	0	0	0	1			1	1	1	1	1	0

Bit(s)	Name	Description
13:8	reg_type_c_cc_src_vrd_30_dac_val	**Type-C CC Source VRD 30 DAC value** The value to for DAC to compare Source VRD voltage when support 3.0A current
5:0	reg_type_c_cc_src_vopen_30_dac_val	**Type-C CC Source VOPEN 30 DAC value** The value to for DAC to compare Source VOPEN voltage when support 3.0A current

0828 **TYPE_C_CC_SNK_DAC_VAL_0** **TYPE-C CC SNK DAC Value 0** **0E1D**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

0828 **TYPE_C_CC_SNK_DAC_VAL_0** **TYPE-C CC SNK DAC Value 0** **0E1D**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			reg_type_c_cc_snk_vrp15_dac_val								reg_type_c_cc_snk_vrp30_dac_val					
Type			RW								RW					
Reset			0	0	1	1	1	0			0	1	1	1	0	1

Bit(s)	Name	Description
13:8	reg_type_c_cc_snk_vrp15_dac_val	**Type-C CC Sink VRP15 DAC value** The value to for DAC to compare Sink VRP15 voltage
5:0	reg_type_c_cc_snk_vrp30_dac_val	**Type-C CC Sink VRP30 DAC value** The value to for DAC to compare Sink VRP30 voltage

082A **TYPE_C_CC_SNK_DAC_VAL_1** **TYPE-C CC SNK DAC Value 1** **0002**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											reg_type_c_cc_snk_vrpusb_dac_val					
Type											RW					
Reset											0	0	0	0	1	0

Bit(s)	Name	Description
5:0	reg_type_c_cc_snk_vrpusb_dac_val	**Type-C CC Sink VRPUSB DAC value** The value to for DAC to compare Sink VRPUSB voltage

0830 **TYPE_C_INTR_EN_0** **TYPE-C Interrupt Enable 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	reg_type_c_cc_ent_dbg_acc_snk_intr_en	reg_type_c_cc_ent_dbg_acc_src_intr_en	reg_type_c_cc_ent_try_wait_src_intr_en	reg_type_c_cc_ent_try_snk_intr_en	reg_type_c_cc_ent_attach_wait_acc_intr_en	reg_type_c_cc_ent_unattach_acc_intr_en	reg_type_c_cc_ent_try_wait_snk_intr_en	reg_type_c_cc_ent_try_src_intr_en	reg_type_c_cc_ent_attach_wait_snk_intr_en	reg_type_c_cc_ent_attach_wait_src_intr_en	reg_type_c_cc_ent_unattach_snk_intr_en	reg_type_c_cc_ent_unattach_src_intr_en	reg_type_c_cc_ent_disable_intr_en	reg_type_c_cc_ent_audio_acc_intr_en	reg_type_c_cc_ent_attach_snk_intr_en	reg_type_c_cc_ent_attach_src_intr_en
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	reg_type_c_cc_ent_dbg_acc_snk_intr_en	**Type-C CC enter debug accessory SNK interrupt enable.** Enable type_c_cc_ent_debug_acc_snk_intr interrupt.

Bit(s)	Name	Description
14	reg_type_c_cc_ent_dbg_acc_src_intr_en	**Type-C CC enter debug accessory SRC interrupt enable.** Enable type_c_cc_ent_debug_acc_src_intr interrupt.
13	reg_type_c_cc_ent_try_wait_src_intr_en	**Type-C CC enter TryWait.SRC state interrupt enable.** Enable type_c_cc_ent_try_wait_src_intr interrupt.
12	reg_type_c_cc_ent_try_snk_intr_en	**Type-C CC enter Try.SNK state interrupt enable.** Enable type_c_cc_ent_try_snk_intr interrupt.
11	reg_type_c_cc_ent_attach_wait_acc_intr_en	**Type-C CC enter AttachWait.Accessory state interrupt enable.** Enable type_c_cc_ent_attach_wait_acc_intr interrupt.
10	reg_type_c_cc_ent_unattach_acc_intr_en	**Type-C CC enter Unattach.Accessory state interrupt enable.** Enable type_c_cc_ent_unattach_acc_intr interrupt.
9	reg_type_c_cc_ent_try_wait_snk_intr_en	**Type-C CC enter TryWait.SNK state interrupt enable.** Enable type_c_cc_ent_try_wait_snk_intr interrupt.
8	reg_type_c_cc_ent_try_src_intr_en	**Type-C CC enter Try.SRC state interrupt enable.** Enable type_c_cc_ent_try_src_intr interrupt.
7	reg_type_c_cc_ent_attach_wait_snk_intr_en	**Type-C CC enter AttachWait.SNK state interrupt enable.** Enable type_c_cc_ent_attach_wait_snk_intr interrupt.
6	reg_type_c_cc_ent_attach_wait_src_intr_en	**Type-C CC enter AttachWait.SRC state interrupt enable.** Enable type_c_cc_ent_attach_wait_src_intr interrupt.
5	reg_type_c_cc_ent_unattach_snk_intr_en	**Type-C CC enter Unattach.SNK state interrupt enable.** Enable type_c_cc_ent_unattach_snk_intr interrupt.
4	reg_type_c_cc_ent_unattach_src_intr_en	**Type-C CC enter Unattach.SRC state interrupt enable.** Enable type_c_cc_ent_unattach_src_intr interrupt.
3	reg_type_c_cc_ent_disable_intr_en	**Type-C CC enter Disable state interrupt enable.** Enable type_c_cc_ent_disable_intr interrupt.
2	reg_type_c_cc_ent_audio_acc_intr_en	**Type-C CC enter audio accessory interrupt enable.** Enable type_c_cc_ent_audio_acc_intr interrupt.
1	reg_type_c_cc_ent_attach_snk_intr_en	**Type-C CC enter attach Sink interrupt enable.** Enable type_c_cc_ent_attach_snk_intr interrupt.
0	reg_type_c_cc_ent_attach_src_intr_en	**Type-C CC enter attach Source interrupt enable.** Enable type_c_cc_ent_attach_src_intr interrupt.

0834 **TYPE_C_INTR_EN_2** **TYPE-C Interrupt Enable 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												reg_type_c_cc_ent_snk_pwr	reg_type_c_cc_ent_snk_pwr	reg_type_c_cc_ent_snk_pwr	reg_type_c_cc_ent_snk_pwr	reg_type_c_cc_ent_snk_pwr

0834 **TYPE_C_INTR_EN_2** **TYPE-C Interrupt Enable 2** **0000**

												_redetect_intr_en	_3o_intr_en	_15_intr_en	_default_intr_en	_idle_intr_en
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	reg_type_c_cc_ent_snk_pwr_redetect_intr_en	**Type-C CC enter sink power redetect current sate interrupt enable.** Enable type_c_cc_ent_snk_pwr_redetect interrupt.
3	reg_type_c_cc_ent_snk_pwr_30_intr_en	**Type-C CC enter sink power 3.0A current sate interrupt enable.** Enable type_c_cc_ent_snk_pwr_30 interrupt.
2	reg_type_c_cc_ent_snk_pwr_15_intr_en	**Type-C CC enter sink power 1.5A current sate interrupt enable.** Enable type_c_cc_ent_snk_pwr_15 interrupt.
1	reg_type_c_cc_ent_snk_pwr_default_intr_en	**Type-C CC enter sink power default current sate interrupt enable.** Enable type_c_cc_ent_snk_pwr_default interrupt.
0	reg_type_c_cc_ent_snk_pwr_idle_intr_en	**Type-C CC enter sink power idle sate interrupt enable.** Enable type_c_cc_ent_snk_pwr_idle interrupt.

0838 **TYPE_C_INTR_0** **TYPE-C Interrupt 0** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	type_cc_ent_dbg_acc_snk_intr	type_cc_ent_dbg_acc_src_intr	type_cc_ent_try_wait_src_intr	type_cc_ent_try_snk_intr	type_cc_ent_attach_wait_acc_intr	type_cc_ent_unattach_acc_intr	type_cc_ent_try_wait_snk_intr	type_cc_ent_try_src_intr	type_cc_ent_attach_wait_snk_intr	type_cc_ent_attach_wait_src_intr	type_cc_ent_unattach_snk_intr	type_cc_ent_unattach_src_intr	type_cc_ent_disable_intr	type_cc_ent_audio_acc_intr	type_cc_ent_attach_snk_intr	type_cc_ent_attach_src_intr
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	type_c_cc_ent_dbg_acc_snk_intr	**Type-C CC enter DebugAccessorySNK state interrupt.** Set when CC enter DebugAccessorySNK state.
14	type_c_cc_ent_dbg_acc_src_intr	**Type-C CC enter DebugAccessorySRC state interrupt.** Set when CC enter DebugAccessorySRC state.
13	type_c_cc_ent_try_wait_src_intr	**Type-C CC enter TryWait.SRC state interrupt.** Set when CC enter TryWait.SRC state.

Bit(s)	Name	Description
12	type_c_cc_ent_try_snk_intr	**Type-C CC enter Try.SNK state interrupt.** Set when CC enter Try.SNK state.
11	type_c_cc_ent_attach_wait_acc_intr	**Type-C CC enter AttachWait.Accessory state interrupt.** Set when CC enter AttachWait.Accessory state.
10	type_c_cc_ent_unattach_acc_intr	**Type-C CC enter Unattach.Accessory state interrupt.** Set when CC enter Unattach.Accessory state.
9	type_c_cc_ent_try_wait_snk_intr	**Type-C CC enter TryWait.SNK state interrupt.** Set when CC enter TryWait.SNK state.
8	type_c_cc_ent_try_src_intr	**Type-C CC enter Try.SRC state interrupt.** Set when CC enter Try.SRC state.
7	type_c_cc_ent_attach_wait_snk_intr	**Type-C CC enter AttachWait.SNK state interrupt.** Set when CC enter AttachWait.SNK state.
6	type_c_cc_ent_attach_wait_src_intr	**Type-C CC enter AttachWait.SRC state interrupt.** Set when CC enter AttachWait.SRC state.
5	type_c_cc_ent_unattach_snk_intr	**Type-C CC enter Unattach.SNK state interrupt.** Set when CC enter Unattaach.SNK state.
4	type_c_cc_ent_unattach_src_intr	**Type-C CC enter Unattach.SRC state interrupt.** Set when CC enter Unattach.SRC state.
3	type_c_cc_ent_disable_intr	**Type-C CC enter Disable state interrupt.** Set when CC enter Disable state.
2	type_c_cc_ent_audio_acc_intr	**Type-C CC enter AudioAccessory state interrupt.** Set when CC enter AudioAccessory state.
1	type_c_cc_ent_attach_snk_intr	**Type-C CC enter Attach.SNK state interrupt.** Set when CC enter Attach.SNK state.
0	type_c_cc_ent_attach_src_intr	**Type-C CC enter Attach.SRC state interrupt.** Set when CC enter Attach.SRC state.

083C **TYPE_C_INTR_2** **TYPE-C Interrupt 2** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												type_c_cc_ent_snk_pwr_redetect_intr	type_c_cc_ent_snk_pwr_3o_intr	type_c_cc_ent_snk_pwr_15_intr	type_c_cc_ent_snk_pwr_default_intr	type_c_cc_ent_snk_pwr_idle_intr
Type												W1C	W1C	W1C	W1C	W1C
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	type_c_cc_ent_snk_pwr_redetect_intr	**Type-C CC enter sink power redetect current state inerrupt** Set when enter Redetect.SNK state.

Bit(s)	Name	Description
3	type_c_cc_ent_snk_pwr_30_intr	**Type-C CC enter sink power 3.0A current state inerrupt** Set when enter Power3.0.SNK state.
2	type_c_cc_ent_snk_pwr_15_intr	**Type-C CC enter sink power 1.5A current state inerrupt** Set when enter Power1.5.SNK state.
1	type_c_cc_ent_snk_pwr_default_intr	**Type-C CC enter sink power default current state inerrupt** Set when enter PowerDefault.SNK state.
0	type_c_cc_ent_snk_pwr_idle_intr	**Type-C CC enter sink power idle state inerrupt** Set when enter Sink Power Idle state.

0840 **TYPE_C_CC_STATUS** **TYPE-C CC Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ro_type_c_routed_cc												ro_type_c_cc_st			
Type	RU												RU			
Reset	0												0	0	0	0

Bit(s)	Name	Description
15	ro_type_c_routed_cc	**Type-C routed CC** Valid in SRC.Attach or SNK.attach state 1'b0: cc1 1'b1: cc2
3:0	ro_type_c_cc_st	**Type-C CC state.** 4'd0: Disable 4'd1: Unattached Source 4'd2: Attach Wait Source 4'd3: Attach Source 4'd4: Unatched Sink 4'd5: Attach Wait Sink 4'd6: Attach Sink 4'd7: Try Source 4'd8: Try Wait Sink 4'd9: Unattached Accessory 4'd10: Attach Wait Accessory 4'd11: Audio Accessory 4'd12: Debug Accessory Others: Unused

0842 **TYPE_C_PWR_STATUS** **TYPE-C Power Status** **0000**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ro_ad_cc_vusb33	ro_type_c_ad_cc	ro_type_c_drive	ro_type_c_cc_p		ro_type_c_cc_snk_pwr_st		

0842	TYPE_C_PWR_STATUS	TYPE-C Power Status	0000

									_rdy	_cmp_out	_vconn_capable	wr_role				
Type									RU	RU	RU	RU		RU		
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7	ro_ad_cc_vusb33_rdy	**AD CC VUSB33 ready** 1'b0: VUSB33 not ready yet 1'b1: VUSB33 ready Default value depends on current VUSB33 status
6	ro_type_c_ad_cc_cmp_out	**Type-C AD comprator output result** 1'b0: CC voltage < DAC out 1'b1: CC voltage > DAC out
5	ro_type_c_drive_vconn_capable	**Type-C capable to drive VCONN** 1'b0: Can not drive 1'b1: Can drive According to SPEC, first attach Source a. Drive Vconn when other CC pin in SRC.Ra for tCCDebounce. SW must read this CSR before drive VCONN b. Drive Vconn unconditionaly. SW no need to read this CSR. Only valid in Attach.SRC state & enter thsi state from AttachWait.SRC state.
4	ro_type_c_cc_pwr_role	**Type-C power role.** Only work at attach state. 1'b0: Sink 1'b1: Source
2:0	ro_type_c_cc_snk_pwr_st	**Type-C Sink power state.** 3'd0: Sink Power Idle 3'd1: Sink Power Defaule 3'd2: Sink Power 1.5A 3'd3: Sink Power 3.0A 3'd3: Sink Power redetect

5 Application Notes

5.1 Hardware External Shutdown

The schematic below illustrates the hardware external shut-down function for MT6392 to power down when the main chip software crashes.

- Short press PWRKEY or FCHR_ENB
  INT-> EINT -> software control
  Power-down, sleep mode or the other functions

- Long press shut-down
  Force power-off of PMU
  5/8(default)/11/14 s with +/-20% accuracy
  External reset function with source from:
  PWRKEY and FCHR_ENB both pressed for long period of time
  PWRKEY and FCHR_ENB doesn't use same key
  PWRKEY pressed for long period of time (Default)
  FCHR_ENB pressed for long period of time

- Re-start
  System will re-power on if keep long press PWRKEY after system shutdown

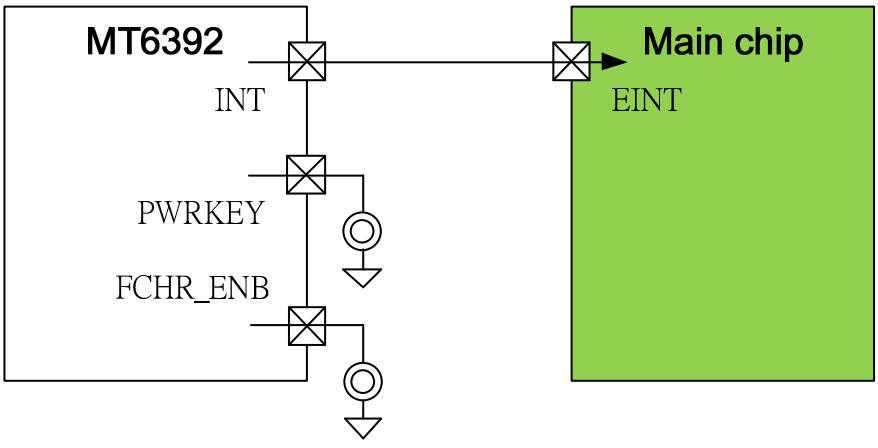


Figure 5-1. Hardware external shut-down function

5.2 Configuration for Unused Buck Converter

The figure below shows the configuration for MT6392 VPROC buck converter that is not used.

- Configuration for VPROC not in use:
  VBAT_VPROC connect to VBAT;
  GND_VPROC connect to GND;
  VPROC_FB: Connect to VIO18;
  GND_VPROC_FB connect to GND;
  VPROC_LX: Floating;
  RG_PROC_EN = 0 & RG_PROC_NDIS_EN = 1

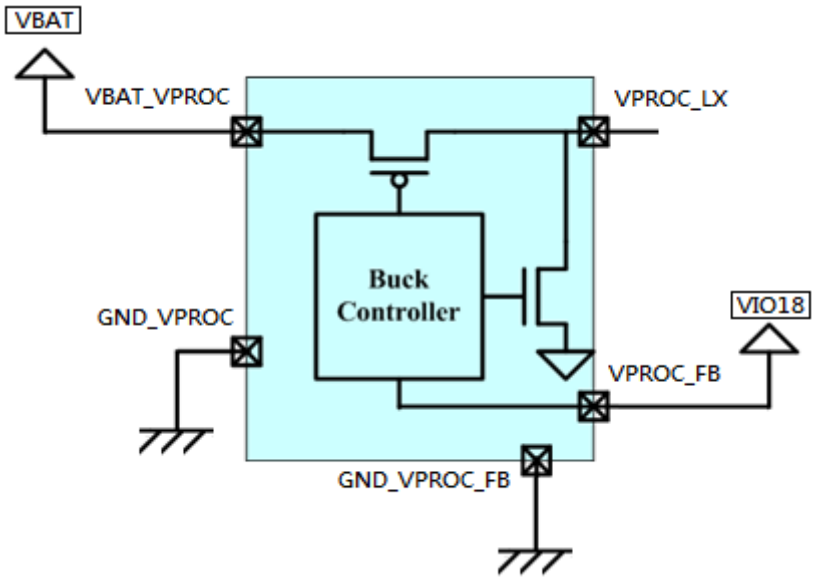
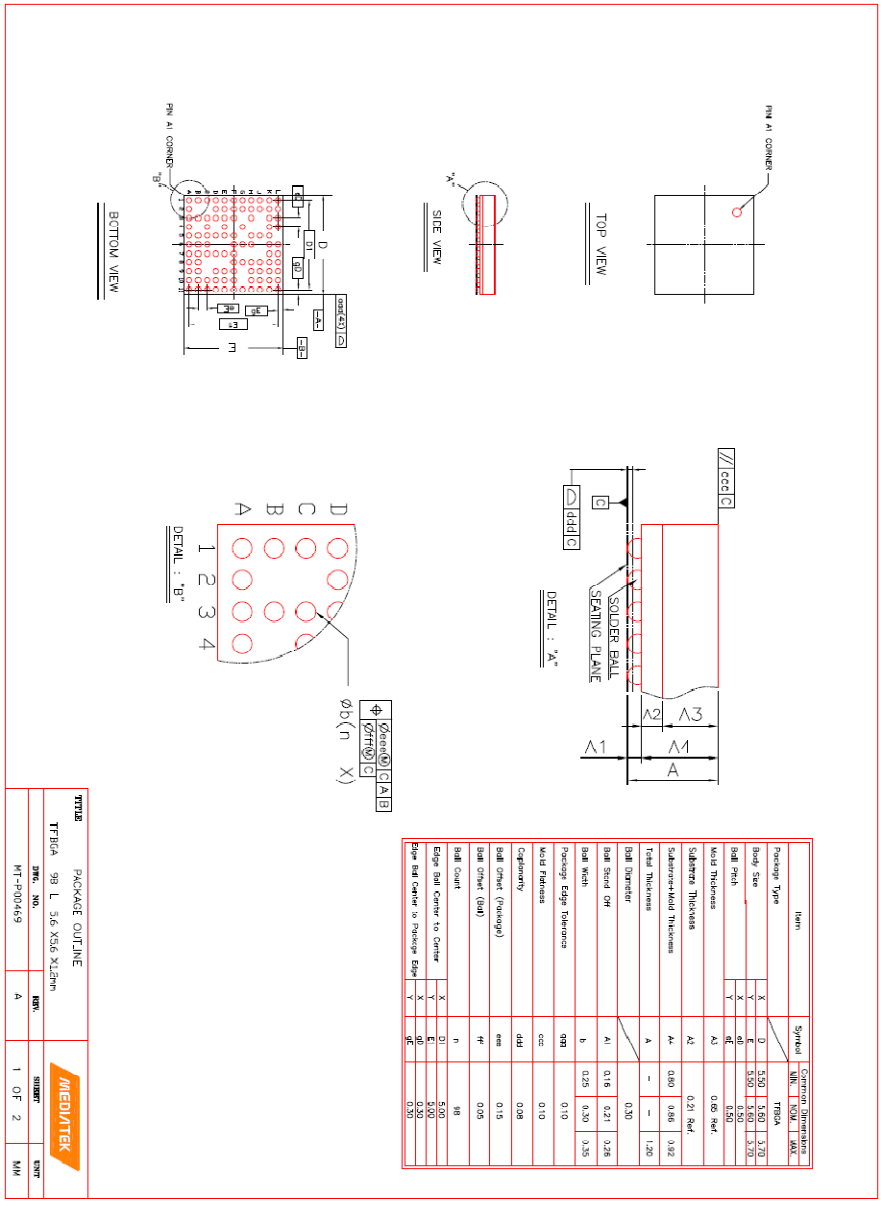


Figure 5-2. Configuration for unused DC/DC

6 MT6392 Packaging

6.1 Package Dimensions



Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type				TFBGA	
Body Size	X	D	5.50	5.60	5.70
	Y	E	5.50	5.60	5.70
Ball Pitch	X	eD		0.50	
	Y	eE		0.50	
Mold Thickness		A3		0.21 Ref.	
Substrate Thickness		A2		0.21 Ref.	
Substrate+Mold Thickness		A+	0.80	0.86	0.92
Total Thickness		A	–	–	1.20
Ball Diameter				0.30	
Ball Stand Off		A1	0.16	0.21	0.26
Ball Width		b	0.25	0.30	0.35
Package Edge Tolerance		aaa		0.10	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		98	
Edge Ball Center to Center	X	eD		5.00	
	Y	eE		5.00	
Edge Ball Center to Package Edge	X	sD		0.30	
	Y	sE		0.30	

6.2 Package Details

ITEM		Symbol	Common Dimensions		
			Min	Nom	Max
Package Type			TFBGA		
Body Size	X	D	5.50	5.60	5.70
	Y	E	5.50	5.50	5.70
Ball Pitch	X	eD	.50		
	Y	eE	.50		
Mold Thickness		A3	.65 Ref.		
Substrate Thickness		A2	.21 Ref.		
Substrate + Mold Thickness		A4	0.80	0.86	0.92
Total Thickness		A	-	-	1.20
Ball Diameter			0.30		
Ball Stand Off		A1	0.16	0.21	0.26
Ball Width		b	0.25	0.30	0.35
Package Edge Tolerance		aaa	0.10		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	98		
Edge Ball Center to Center	X	D1	5.0		
	Y	E1	5.0		
Edge Ball Center to Packaging	X	gD	0.30		
	Y	gE	0.30		

